Wayne P. Burleson

Citizenship: U.S.A.
Marital Status: Married, Four children (ages 14, 11, 8, 5)
Birth date: July 3, 1960, Seattle, Washington

ADDRESSES
Office:
Knowles Engineering Building, 309C
Department of Electrical and Computer Engineering
University of Massachusetts
Amherst, MA 01003-5110
tel: (413) 545-2382
fax: (413) 545-1993
email: burleson@ecs.umass.edu
WWW: http://www.ecs.umass.edu/ece/vspgroup/burleson.html
Office manager: (Christine Langlois) 413-545-3621
Home:
84 Leonard Rd.
Shutesbury, MA 01002
(413) 259-9995

EDUCATION

PHD in Electrical Engineering, **University of Colorado**, Boulder, CO. 12/89.
Thesis: Efficient Computation in VLSI with Distributed Arithmetic.
Advisor: Professor Louis L. Scharf

MSEE **Massachusetts Institute of Technology**, Cambridge, MA. 6/83.
Thesis: A Programmable Bit-serial Signal Processing Chip.
Advisors: Professor Campbell L. Searle and Richard F. Lyon (Fairchild).

BSEE **Massachusetts Institute of Technology**, Cambridge, MA. 6/83.
(completed simultaneously with MSEE in 5 years in VI-A co-op program)

EMPLOYMENT

9/05-present **University of Massachusetts Amherst**,
Professor of Electrical and Computer Engineering.

9/10-5/11 **Ecole Polytechnique Federale de Lausanne (EPFL), SWITZERLAND**,
Visiting Professor of Electrical Engineering. Research in 3D VLSI and RFID Circuits

9/98-3/11 **Intel Corporation, Massachusetts Microprocessor Design Center, (formerly Alpha Development Group of Digital, Compaq, HP)**, Shrewsbury/Hudson, MA.
Consultant on on-chip sensing, soft-errors, clocking, interconnect circuits, low power and design techniques for advanced microprocessors.

9/96-8/05 **University of Massachusetts Amherst**,
Associate Professor of Electrical and Computer Engineering.
Research in the Design and Implementation of Signal Processing and Communication Systems.

Research in Advanced CMOS Circuit Design. Development of Multimedia Courseware, Educational Co-Director of CASA, an NSF Engineering Research Center.
Teaching of VLSI Design, VLSI Design Project, Embedded Systems Design, Multimedia Systems and Introduction to Programming.

9/03-12/03 **University of Montpellier II, France, Laboratoire des Informatique, Robotique et Microelectronique (LIRMM)**. Montpellier, FRANCE
Visiting researcher on the topics of on-chip interconnect modeling and reconfigurable computing.

7/01-2/05 **National Technological University** (now a division of Laureate Inc. On-line Higher Education), Baltimore, MD.
Curriculum Chair of Computer Engineering, member of Academic Executive Committee.

5/00-8/10 **Datafusion/Tensorcomm Corporations**, Northglenn, CO.
Consultant on cryptography, cellular and GPS implementations in ASIC, FPGA and DSP.

9/96-8/97 **Ecole Nationale Superieure des Telecommunications, Paris, France**.
Sabbatical leave as a visiting professor in the Departmente Electronique.
Research in Adaptive VLSI for Wireless Communications. Innovative teaching involving Internet-based embedded system design project between ENST/Paris, UMASS/Amherst and Pusan National University, South Korea.

9/90-8/96 **University of Massachusetts, Amherst**
Assistant Professor of Electrical and Computer Engineering.
Conducted NSF-funded research in VLSI Timing Design, Array Architectures for DSP/Arithmetic and Computer-Aided Design. Developed new courses in Embedded Systems, VLSI Architecture, VLSI for Digital Signal Processing and VLSI Logic Synthesis. Developed new curricula for VLSI Design sequence, Digital Design and HW Organization. Developed video short courses in VHDL/Verilog and Computer Systems Manufacturing.

1/87-8/90 **University of Colorado,** Boulder, CO.
Research assistant in digital signal processing laboratory. Work involved development of a design methodology for decomposing DSP algorithms at the bit level leading to highly parallel VLSI implementations. Included full-custom design of a 138,000 transistor CMOS chip. Funding provided by Ball Aerospace and ONR.

8/86-12/86 **University of Colorado,** Boulder, CO.
Teaching assistant in circuits and communications laboratories.

8/83-8/86 **VLSI Technology Inc.**, San Jose, CA.
Architecture, instruction set design and implementation of a CMOS signal processing chip for telecommunications applications. Full-custom design of address generation hardware, internal bus interface and instruction cache and decoder. Architectural specification and design of a CMOS signal processor. Work on this 120,000 transistor chip involved instruction set, logic and circuit design with extensive simulation at all levels. Specific tasks included design of an instruction cache, multi-port register files and a fast hardware implementation of transcendental functions (see Patents).

1/83-5/83 **Massachusetts Institute of Technology**, Cambridge, MA.
Teaching assistant for a course in circuits and network theory.

6/82-1/83 **Fairchild Research and Development**, Palo Alto, CA.

Design and layout of a special purpose signal processing chip in an NMOS technology. Involved design and simulation at the functional, logic and circuit level. Chip was functional on first silicon prototype. (see Master's thesis)

6/81-8/81 **Fairchild Research and Development**, Palo Alto, CA.
Design and simulation of bipolar SRAM cells. Extensive use of SPICE for analog simulation.

HONORS AND AWARDS

2011 **IEEE Fellow** for contributions to integrated circuit design and signal processing

2004-5 Nominated for the University Distinguished Teaching Award

2004 Certificate of Appreciation Award for Demonstrating Excellence in Teaching as Evaluated by Students in EDUC 691JJ, Engineering Complex Systems for Classroom Teachers, Summer 2004.

1999 Ben Dasher Award for **Best Paper** at the 1999 Frontiers in Education Conference, the leading IEEE/ASEE sponsored engineering education conference. Paper was chosen from 400 presented papers. Award was based on both paper and oral presentation given by Burleson. Paper title: *Educational Innovations in Multimedia Systems*, W. Burleson, A. Ganz, I. Harris.

1996 **Outstanding Junior Faculty Member**,
College of Engineering, University of Massachusetts, Amherst.

1996, 1995, 1994, 1993: **Outstanding Faculty Contribution to IEEE Student Branch**, University of Massachusetts, Amherst.

1993 Massachusetts Microelectronics Center VLSI Design Contest (supervised both first and second place student teams)

1992 **Outstanding Professor Award** ,
ECE Department, University of Massachusetts, Amherst.
(chosen by UMASS ECE undergraduates for teaching excellence and service to students)

1992 Cadence Design Systems University Research Award, $1000 (chosen based on university research using Cadence VLSI tools)

1992 Massachusetts Microelectronics Center VLSI Design Contest (supervised both first and second place student teams)

1991 National Science Foundation **Research Initiation Award**, $60,000
“Designing VLSI Arithmetic Arrays to Satisfy Precision Constraints".

RESEARCH SUMMARY

Dr. Burleson has been working in the area of VLSI Design since 1982. His work has included research, development, teaching and industrial work at a variety of levels including theory, algorithms, architectures, circuits and CAD tools. Dr. Burleson is currently Professor of Electrical and Computer Engineering at the University of Massachusetts at Amherst where he has been since 1990. He received his BSEE and MSEE from MIT in 1983 and his PhD from the University of Colorado, 1989. He worked as a custom DSP chip designer for 4 years for VLSI Technology Inc. and Fairchild Semiconductor. He has consulted with Intel, Compaq, HP, Tensorcomm and Datafusion. He was a visiting professor at the Ecole Nationale Superieure des Telecommunications in Paris from September 1996 to August 1997 and with the Laboratoire de Informatique, Robotique et Microelectronique (LIRMM) de Montpellier in Fall of 2003. He is a Fellow of the IEEE for contributions in integrated circuit design and signal processing, and a member of ASEE, ACM and Sigma Xi.

Prof. Burleson has conducted VLSI and DSP research funded by NSF, SRC, Sharp and Intel and has published over 170 journal and conference papers in the following areas: Reconfigurable Communications, VLSI for Communications and Digital Signal Processing; Low-Power Design, Hardware Emulation of Real-Time Systems; Co-design and co-verification of Hardware-Software Systems; Computer Arithmetic, VLSI for Data Compression, Error-Correction, Cryptography, RFID Systems, Scheduling, Path Control, Protocols; Bit-level Algorithms and Mappings to VLSI and FPGA Architectures. Prof. Burleson also leads research in engineering education funded by NSF. He was the education co-director of an NSF Engineering Research Center at UMASS. He is currently developing a multi-disciplinary research group in the area of Embedded Security with applications in Transportation, Supply Chain, Medical and Government.

Prof. Burleson's research stands out in the following ways:

- Transcending levels of abstraction in circuits, source coding, communications systems, imaging, video and 3D graphics content coding.
    - New highly pipelined architectures derived with systematic methodologies,
    - Accounting for deep sub-micron effects like interconnect, power and soft-errors,
    - Exploiting application characteristics, especially in terms of human perception of video and 3D graphics
- Questioning standard design assumptions:
    - timing optimization, new signaling and sense-amp designs for high-speed and low-power
    - on-chip signaling (bus-coding and current vs. voltage signaling)
    - wave-pipelining, (timing structures)
    - data compression, (lossless and lossy approaches)
    - re-purposing existing resources (e.g. SRAM for Chip ID and Random Number Generation)
    - hardware support for cryptography, 3D graphics rendering, real-time scheduling, path planning, etc.
- Spreading the word of appropriate roles of technology in education at all levels
    - K12 curriculum development (outreach, and frameworks)
    - K12 infrastructure development (weather stations, remote sensing, etc.)
    - Undergraduate engineering curriculum to encouragement recruitment of under-represented groups.
    - Undergraduate engineering opportunities to engage in research.

GRADUATE STUDENTS

Current PhD Students:

1. Ibis Benito: VLSI Interconnect Circuit Design
2. Georg Becker: Secure Component Identification with Intentional Side-Channels (co-advised with C. Paar)
3. Gesine Hinterwalder: Lightweight Elliptic Curve Implementations (co-advised w/ C. Paar)
4. Xaolin Xu: Hardware Security
5. Raghavan Kumar: Physical Unclonable Functions
6. Vikram Suresh: True Random Number Generation

Current MS Students:

1. Vinay Patel: 3D Power Supply Modeling
2. GireeshVijayakumar: On-Chip Sensors

Ph.D. Graduates:

1. Lang Lin: Cryptography in Nanometer CMOS (now at Intel)
2. Basab Datta: Thermal Effects and On-Chip Sensors (now at AMD)
3. Jinwook Jang: Jitter in On-Chip Interconnects (took position at AMD)
4. Vishak Venkatraman, Multi-level Current Signaling, took position at AMD
5. Matt Heath: Synchro-tokens, took position at Intel
6. Atul Maheshwari: Current-mode Circuits for Long Interconnects , took position at Intel
7. Capt. Andrew Laffely: Configurable Computing for Low-Power Signal Processing, took faculty position at Hanscomb Air Force Base.
8. Jeongseon Euh: took position at Samsung Semiconductor, Portable Products Group
9. Mircea Stan, took position at University of Virginia, now Associate Professor (NSF/CAREER Award)
10. Bongjin Jung, took position as Senior Engineer at Intel
11. Yongjin Jeong took position at Samsung, now Associate Professor at Kwangwoon University, South Korea
12. Taek-Soo Kim, now Manager at Samsung Semiconductor
13. Hyunhee Choi took position as Senior VLSI Designer at Advanced Micro Devices
14. Zheng Zhou took position as CAD Researcher at Silicon Graphics Inc.

M.Sc. thesis Graduates:

1. Vikram Suresh: True Random Number Generation
2. Sudheendra Srivaths: Physically Unclonable Functions in Nanometer CMOS
3. Ashwin Lakshminarsinham: EM Side-Channel Analysis for Watermarking (now at Intel)
4. Krishna Chillara: Signal Techniques for Through-Silicon Vias (now at Intel)
5. Mike Todd: Hardware Emulation of Secure RFID Sensors (now at Intel, AZ))
6. Serge Zhilyaev: Applied Cryptography for RFID (took position at Intel, AZ)
7. Xiang Yun: Thermal Sensor Placement (pursuing PhD at U. Michigan)
8. Lang Lin: Leakage-based Power Analysis (continuing in PhD program with Burleson)

9. Venkatesh Arunachalam (Clock Distribution in 3D Microprocessor), (took position at SUN Microsystems)
10. Ibis Benito: Global Interconnects in the Presence of Uncertainty, (continuing in UMass PhD program)
11. Dan Holcomb: SRAM for Chip ID and TRNG (continuing in UC Berkeley Phd program)
12. Basab Datta: Thermal Sensors (continuing in UMASS PhD program)
13. Sheng Xu: Current-sensed interconnects (took position at Analog Devices)
14. Jinwook Jang (Jitter in On-Chip Interconnects) (continuing in UMass PhD program)
15. Chris Cowell: Interconnect-driven Architectural Performance optimization (took position at Intel)
16. Aiyappan Natarajan: Content-addressable Memory for Smart Cards (took position at AMD)
17. Jeevan Chittamuru: Content-adaptive Texture-mapping for 3Dgraphics (took position at ..)
18. Vijay Shankar: Leakage and Variations in On-Chip Caches (took position at Qualcomm)
19. Srividya Srinivasaraghavan: Interconnect Effort (took position at Intel)
20. Sriram Srinivasan: Current-mode Circuits for Long Interconnects (took position at AMD)
21. Manoj Sinha: Current-mode Circuits for RAMs (took position at Micron)
22. Santosh Thampuram: CD/DVD-based Distance Learning Technology (took position at Bloomburg)
23. Atul Maheshwari: Current-mode Circuits for Long Interconnects: (took position UMASS PhD)
24. Prashant Jain: Content-Aware Low-power VLSI Video Coding (took position UMASS PhD)
25. Subramanian Venkatraman: Power-Aware DSP Architectures and Tools (took position at Intel)
26. Chandrika Duggirala: Tools to Support Flexible Modular Curricula (took position at Motorola)
27. Anki Nalamalpu , Repeater Design in DSM CMOS (took position at Intel, Hillsboro, MA)
28. Nitin Srimal, Indexing of Hand-written text and Video. (took position in PhD program at U. Michigan.)
29. Jason Ko, Scheduling Co-processor (VLSI Designer, Hewlett Packard, CA)
30. Bongjin Jung, Array Estimation and Simulation CAD Tools (took position at Intel)
31. Sashi Obilisetty, (founder and CEO of DualSoft, Nashua, NH, since acquired by TransEDA)
32. Yamini Polisetty, Signal Flow Graph Transformation Tools(took position as CAD Developer, Quantum, MA)
33. Wei-han Lien, Wave-Domino Logic (took position asVLSI Designer, HAL Computer, Sunnyvale, CA)
34. Walter Marvin, CAD for Optical Computing (took position as OS software consultant, CT)

FUNDING

Summary: I have 10 active grants and contracts, with sources including the NSF, SRC, Intel, CISCO, and both Federal and Massachusetts Departments of Transportation, totalling over $4.0 million in funding. Collaborations include Civil Engineering, Computer Science, Brown University, UMass Dartmouth, RSA Labs and Intel.

Current:

Type	Status	Description
Contract	Awarded (NEW)	**Semiconductor Research Corporation (SRC)** *Sub-45nm Circuit Design for True Random Number Generation and Chip Identification*, Co-PI w/ C. Paar, $300,000, 3/1/11-2/31/14.
Contract	Active	**Semiconductor Research Corporation (SRC)** *On-Chip Sensing Strategies for Efficient and Robust Scalability in Many-Core Architectures*, Co-PI w/ R. Tessier, $300,000, 8/1/10-7/31/13.
Grant	Active	**National Science Foundation,** CNS0964641, *TC: Medium: Collaborative Research: Pay-as-you-Go: Security and Privacy for Integrated Transportation Payment Systems*, Lead PI w/ K. Fu, J. Collura, C. Paar and collaborative with Brown University, A. Lysyanskaya, and U. Mass. Dartmouth, M. Zarrillo, total of $1.17 million ($844,997 to UMass), 6/1/10- 5/31/13.
Unrestricted Gift	Active	**CISCO Corporation.** *Alternative Public Key Cryptosystems*, Co-PI w/ C. Paar, $80,000, 9/1/09- open-ended.
Grant	Active	**National Science Foundation:** CNS0923313 *MRI: Acquisition of an RFID Testbed Using Renewable Energy for Object Identification and Habitat Monitoring,* $450,000 w/ Kevin Fu, Yanlei Diao, Prashant Shenoy, 08/01/09-07/31/11.
Grant	Active	**National Science Foundation,** CCF0916854 *TC: Small: Minimalist Hardware Trojans through Malicious Side-Channels* , Co-PI w/ C. Paar, $350,657, 6/1/09-5/31/12.
Grant	Active	**National Science Foundation:** CNS 0831133 *CT-ER: Ultra-wideband Radio for Low-Power Security*, Co-PI w/ D. Goeckel and R. Jackson, $200,000, 9/1/08-8/31/11.
Grant	Active	**US Dept of Transportation** through MIT (Yr 2 Education Project) Co-PI w/ J. Collura. "*Integrated Transportation Payment Systems: Principles, Concepts, and Applications*" $33,914, 09/01/08 - 08/31/11.
Unrestricted gift	Active	**Intel Corporation** "*Multi-bit Temporally Coded Signaling for On-Chip Interconnects*", sole PI .$120,000 6/1/06 - open-ended.

Grant	Active	**National Science Foundation:** CNS0627529 *CT-T Collaborative Research: Security for Smart Tags,* Co-PI w/ K. Fu, UMASS CompSci, Collaborators on the grant include Johns Hopkins University and RSA Labs. $899,000.00 (my share is approximately $395,000, 9/1/06,-8/31/11.

Previous Funding:

UMass President's Office Science and Technology Grant "*Integrated Payment Systems: Security and Privacy*", Co-PI with K. Fu (Computer Science), J. Collura (Civil and Environmental Engineering), M. Zarrillo (Physics, UMASS Dartmouth), $125,000, with matching funds totaling ~ $250,000. 7/1/08-6/30/10.

Massachusetts Executive Office of Transportation
"*An Analysis of Alternative Transportation Financing Approaches: Phase 1*" Co-PI w/ J. Collura $39,042 06/05/07 - 12/31/09. Phase II anticipated in Fall 2011.

Semiconductor Research Corporation: Task 1595 *"Networks of On-Chip Monitors for Run-time Estimation of Power, Reliability and Security*. Co-PI w/ R. Tessier, $300,000, 3/1/07-2/28/10, 3 years

Intel Corporation, "Reliable and Low-Power Adaptive Clocking Systems for Advanced Microprocessors" Co-PI w/ S. Kundu $318,000 , 3/1/06-2/28/09. A collaboration with the Massachusetts Microprocessor Design Center, Hudson, MA.

Semiconductor Research Corporation: Task 1415 "Thermal Sensing and Management in Mobile Microprocessors" Co-PI w/ S. Kundu, $300,000, 6/1/06-5/31/09

Semiconductor Research Corporation Task 1099"Multi-bit Signaling for On-Chip Interconnects", sole-PI, $420,000, April 03- Aug 06.

Semiconductor Research Corporation Task 766 "Current-mode for Global Interconnects", Supplement for Undergraduate Research, sole PI, $24,000 April 03 – Feb 2006 .

Intel Corporation "Current-Sensing Techniques for Advanced Microprocessor Caches", $120,000 Aug 02-July 05. sole PI .

National Collegiate Innovation and Invention Alliance (NCIIA), "Low-cost PC for Developing Nations", Co-PI w/ C. Pal (CompSci), $13,500, 9/1/06-8/31/07

National Science Foundation "Engineering Research Center: Collaborative Adaptive Sensing of the Atmosphere"**,** co-managed education and outreach budget of approximately $200,000 per year for 5 years. August 2003- July 2008- I was not a PI but was a member of the Executive Committee and funded one summer month each year.

Intel Corporation, $120,000, 6/1/02- open-ended. "Advanced Circuits for Microprocessor Caches", Sole PI. Collaboration with Intel CRL, Ram Krishnamurthy, Vivek De.

National Science Foundation, CCR9988238 "Adaptive System on a Chip for Low-Power Signal Processing", w/ R. Tessier, $352,086, 7/1/00-6/30/04.

Semiconductor Research Corporation, $300,000, 2/1/00-1/31/03. "Current-Mode Circuits for Global Interconnects in 70nm CMOS". Sole PI. Collaborations with M. Gowan at Alpha Development Group, Compaq and K. Soumyanath, Intel.

Semiconductor Research Corporation, $24,000, 9/1/00-1/31/03. "Undergraduate Research in: Current-Mode Circuits for Global Interconnects in 70nm CMOS"

Massachusetts Board of Higher Education, Commonwealth Information Technology Initiative (CITI) "Curriculum in Multimedia Systems", $15,000, 1/31/01-8/31/01

Faculty Teaching Grant, **University of Massachusetts** Center for Teaching, "Labs for a new course in Multimedia Systems", $5000, 6/1/00-5/31/01

National Science Foundation EIA 98-12589, "Multimedia Systems: An Integrated Modular Curriculum", lead PI w/ 6 other CSE faculty, $470,000 ($267,000 UMass match), 8/1/98-7/31/02.

National Science Foundation, "Research Experiences for Undergraduates in Multimedia Systems", $12,500, 9/1/00-8/31/02. A supplement to NSF EIA 98-12589.

National Science Foundation, Award No. CDA-9529462, Co-PI with A. Ganz "CISE Instrumentation: Equipment for Real-time Systems Prototyping", $36,000, April 1996 - October 1997.

Faculty Teaching Grant, **University of Massachusetts** Center for Teaching, "International Collaboration for Electronic Design via the World Wide Web", w/ M. Ciesielski, $1,500, 6/1/96-5/31/97.

Professional Development Grant for Instructional Technology in Academic Development. **University of Massachusetts** President's Office, "International Collaboration for Electronic Design via the World Wide Web", w/ M. Ciesielski $4,000, 6/1/96-5/31/97.

National Science Foundation, Award No. MIP-9208267, equal PI with Maciej Ciesielski, "High-Performance VLSI Synthesis with Wave Pipelining" $252,380, Sept. 1992 - July. 1996.

National Science Foundation, Award No. INT-9311863, equal PI with Maciej Ciesielski, "High-Performance VLSI Synthesis with Wave Pipelining" $16,230, June 1994 - June 1996. This award provided funding for international cooperation with our colleagues in Seoul and Pusan, Korea in VLSI research.

Engineering Academy of Southern New England (**NSF**), "Integrating Manufacturing into a Senior Computer Design Lab", w/ G. Fischer, University of Rhode Island, $20,000, 7/1/95-6/30/96.

Engineering Academy of Southern New England (**NSF**), " Multimedia Teaching Materials for Electronic Design Tools", $20,000, 3/1/96-6/30/96.

National Science Foundation, Award No. CDA-9320325, Co-PI with six other faculty in UMASS CSE group. "CISE Instrumentation", Equipment for VLSI testing and workstations. $40,000, April 1994 - October 1995.

National Science Foundation Research Initiation Award, MIP-9108086, "Designing VLSI Arithmetic Arrays to Satisfy Precision Constraints", $60,000, 9/91-2/94.

University of Massachusetts Faculty Research Grant, "ARRSIM - A Graphical Array Simulator". $5,000, 6/91-6/92.

Industrial Donations for Research and Instruction (All donations and discounts resulted from research and education proposals beyond the standard university discounts.)

Cryptography Research Inc., dynamic power analysis workstation and software, $180,000 November 2010.

Intel Corporation, workstations and software $20,000, 2002, 2004

Cadence Design Systems, discount on Verilog and VHDL simulator and synthesis licenses, valued at approximately $50,000. 1992-1995.

Altera, donation of programmable logic development tools and programming hardware, valued at approximately $169,000, 1994-1995.

Atmel, donation of programmable logic development tools and programming hardware, valued at approximately $40,000, 1994-1995.

Microchip, donation of microcontroller development tools and hardware, valued at approximately $9,980, 1995-1996.

Xilinx, donation of FPGA development tools and hardware, valued at approximately $50,000, 1996-1997.

Digital Semiconductor, donation of StrongARM microcontroller development tools and hardware, valued at approximately $25,000, 1997.

Texas Instruments, donation of TMS320C60 DSP Development systems and hardware emulators, valued at approximately $5,000, 1998.

Other Funding

Initiated undergraduate fellowship program for UMass ECE students specializing in VLSI design with funding provided by Alpha Development Group, Compaq Computer Corporation. $6000, Spring 2000.

TEACHING

Awards:

Nominated for the University Distinguished Teaching Award 2004-5

Certificate of Appreciation Award for Demonstrating Excellence in Teaching as Evaluated by Students in EDUC 691JJ, Engineering Compelx Systems for Classroom Teachers, Summer 2004.

Courses Taught :
197H Multimedia Systems (a new course for non-majors)
122 Introduction to Programming in C++ (VIP∗)
221 Digital Logic Design (VIP)
232 Hardware Organization and Design (VIP)
494 Professional Seminar
551 Computer Systems Lab
558/658 Intro to VLSI / VLSI Design Principles (VIP)
559/659 VLSI Design Project
597M Distributed Application Design in Java
664 VLSI Architecture (VIP)
666 Computer Arithmetic (VIP)
697AB Security Engineering
697D VLSI Signal Processing
697D Advanced Topics in VLSI (w/ Ciesielski and Koren)
697G Logic Synthesis
697V VLSI Circuit Design
697W Special Topics in Wireless Communications (co-taught with Wireless Communication Center)
(∗ VIP indicates that the course was also offered live through the Video Instructional Program to off-campus students, and in most cases was also available for several additional semesters as a pre-taped distance education course. 558/658 is also available in a novel CD/DVD format developed here at UMASS)

Significant Curriculum Developments

2009 New course in Security Engineering (ECE 697AB) building on new UMass research in Embedded Security. 40 students from ECE, CompSci and Civil Engineering.

2005 New course in Embedded Computing Systems (ECE354) incorporating new labs with embedded soft processors, sensor DSP, secure networking and low-power design.

2003 Engineering problems for Introduction to C++ 122

2002 New VLSI special topics course 697V (offered on top of required teaching load)

2001 New course in Multimedia Systems for non-majors. New labs and web/CD-based format.

2001 Web-based course for Professional Seminar 494

2001 Distributed Software Development using Java in 597M

2000 WebDVD Modules for Multimedia Systems 197H, a new course for the minor in Information Technology

1999-present Web-based VLSI Project course integrating recent research 559/659

1999 New multi-disciplinary course in Wireless Communications

1998 MIPS Web tutorial and VHDL Web tutorial in 232

1997 International Design project involving Umass, ENST/Paris and Pusan University, Korea

1995 Video short course in VHDL/Verilog

1995 Video short course in Computer System Manufacturing

1995 Field Programmable Logic from Altera, PIC Microcontrollers, Advanced DSPs from Texas Instruments in 551

1994 New course in VLSI Architecture 664

1992 New course in VLSI Logic Synthesis 697G

1991 New course in VLSI Signal Processing 697D

SERVICE TO THE DEPARTMENT, COLLEGE AND UNIVERSITY

ECE Faculty Search Committees on Embedded Systems, Security and Computer Architecture

ECE Committee on Undergraduate Process and Program. 03- present

University Faculty Senate Committee on On-Line Learning and Continuing Education 04-08

Advisory Board Professional Education for Engineering and Applied Science (PEEAS) 02-06

ECE Graduate Curriculum Committee 03-present

ECE Personnel Committee , 09-10, 06-07 (chair), 90-91

Cadence and Synopsys CAD tool liason 2000-present (coordinate licensing, setup and maintanence of commercial CAD tools used by 8 ECE faculty in research and teaching)

ECE Department Accreditation ABET 2000 Task Force 1999- (one of 5 members guiding the department effort toward meeting and measuring newly revised accreditation criteria)

University Task Force on Information Technology Program 2001- present (Steering Committee and Committees on Curriculum and Capstone Course)

ECE Computer Systems Engineering Senior Design Project Review Board 02-03

Massachusetts Teachers Association Bargaining Team on Distance Learning

University Information Technologies Planning Committee 95-97

University Council on Teaching, Learning and Instructional Technology 94-97

ECE Instructional Development Committee 94-99, 03-present

IEEE Student Branch Advisor 93-95: Developed new seminar series. Developed WWW pages for local branch and IEEE region 1.

College of Engineering, Engineering Computer Services (ECS) Advisory Board 92-96

MOSIS VLSI Fabrication Liaison 91- present

ECE Department Head Search Committee 94

CSE Qualifying Exam Committee 90-04 (responsible twice a year for Algorithms exam),

Massachusetts Microelectronics Center Liaison 91-93

College of Engineering Curriculum Committee 91-92

ECE Graduate and Undergraduate Curriculum Committee 91-92

PROFESSIONAL ACTIVITIES

Fellow of IEEE, Member of Signal Processing Society. Member of Circuits and Systems Society, Member of Computer Society, Member since 1984, Senior Member since 2001. Fellow since 2011

Chair of IEEE Signal Processing Society Technical Committee on the Design and Implementation of DSP Systems (DISPS), involves planning and coordination of SIPS workshops, ICASSP reviews, award nominations. 2004-2006.

Steering Committee, Program Committee and Posters Chair for *IEEE Conference on Microelectronic Systems Education (MSE)*, 2003,2005,2007

Associate Editor, *IEEE Transactions on VLSI*, 1998-2003

Associate Editor, *ACM Transactions on the Design Automation of Electronic Systems*, (an on-line journal), 1998-2001

Member of IEEE Signal Processing Society Technical Committee on the Design and Implementation of DSP Systems (DISPS), 97-present

Co-Chair, 1998 IEEE VLSI Signal Processing Workshop, Boston. w/ K. Konstantinides.

Guest Editor Special Issue on Recent Advances in the Design and Implementation of DSP Systems of *the Journal of Signal Processing Systems*, Winter 2000. w/ E. Manolakos

Guest Editor Special Issue on Reconfigurable Computing in DSP Systems of *the Journal of Signal Processing Systems*, Summer 2000. w/ N. Shanbhag

Guest Editor Special Issue on VLSI in Wireless Networks in *ACM Wireless Networks*, Spring 1998. w/ M. Steyaert

Guest Editor Special Issue on Recent Advances in the Design and Implementation of DSP Systems of *the Journal of Signal Processing Systems*, Winter 1998. w/ K. Konstantinides.

Editorial Board of *Journal of VLSI Signal Processing Systems*, 1995-.

Editorial Board of IEEE Press Series on Microelectronic Systems, 1997-

Associate Editor *IEEE Transactions on Circuits and Systems, II*., 1994-95.

Technical Program Co-Chair, 1996 IEEE VLSI Signal Processing Workshop, San Francisco w/ K. Konstantinides

Program Committees: ISCAS 95,96; VSP 94,96; SIPS 01, ASAP 94,95,96,97,00,02; TAU 95, ISLPED 97,98

Organizer of a Forum on Wave-pipelining at the 1994 IEEE International Symposium on Circuits and Systems.

Member of Association of Computing Machinery 95-

Member of Sigma Xi 83-

INVITED TALKS

Keynote of SOC-SIC Colloquim, Lyon, France, "Hardware Security in Nanometer CMOS", June 2011.

IMEC, Belgium "On-Chip Sensors: An Enabling Technology for Multi-core and 3D integration", April 2011.

Keynote, Workshop on CMOS Variability, Grenoble, France "On-Chip Sensors: An Enabling Technology for Multi-core and 3D integration", May 2011.

IEEE Medical and Communication Technology, Montreux, Switzerland, "Physical Security with Ultra Wideband". March 2011. **(Invited Talk)**

ETHZ, Zurich, Switzerland, "Lightweight Security and Privacy for Implantable Medical Devices", April 2011.

ENST, Paris, France, "Hardware Security in Nanometer CMOS", April 2011

LIRM, Montpelier, France, "Hardware Security in Nanometer CMOS", February 2011

Ecole des Mines, Gardanne, France, "Hardware Security in Nanometer CMOS", February 2011

EPFL EE Summer School, "Hardware Security in Nanometer CMOS", June 2011

University Jean Monnet, St. Etienne, France, "Hardware Security in Nanometer CMOS", December 2010.

ETHZ, Zurich, Switzerland. "Hardware Security in Nanometer CMOS", December 2010.

CSEM, Neuchatel, Switzerland, "Hardware Security in Nanometer CMOS", November 2010.

Ruhr University, Bochum, Germany, "Hardware Security in Nanometer CMOS", October 2010.

KU Leuven, Belgium , "Hardware Security in Nanometer CMOS", October 2010.

EPFL, Lausanne, Switzerland, "Hardware Security in Nanometer CMOS", October 2010.

Eurecom/ENST, Sophia Antipolis, France, "RFID Innovations at the Bottom", June 2009.

EPFL, Lausanne, Switzerland, "Thermal Sensing and Management", May 2009.

Intel Fault Aware Computing Group, "On-Chip Sensors: A Survey", March 2009.

Intel Circuits Research Lab, Hillsboro, OR, "CMOS Computation in the Presence of Uncertainty: Modelling, Measuring, and Mitigating Variations", September, 2008

Intel Fault Aware Computing Group, "NBTI Wearout: Models, Measurements and Mitigation", March 2008.

EPFL, Lausanne, Switzerland, "Statistical Interconnect Design", June 2006.

ENST/Nice, France, "RFID Security and Privacy: A Hardware Perspective", June 2006

U. of Patras, Patras Greece, "Circuits and Architectures for On-Chip Interconnects",May 2005.

Intel, Hudson, MA "Parity Prediction Circuits", April 2005.

Keynote Address at Boston Area Architecture Conference, Brown University, " Performance, Energy and Reliability Tradeoffs in Deep Sub-Micron CMOS VLSI", January 2005.

Chalmers University, Sweden, “Circuits for Long On-Chip Interconnects”, December 2003.

LIRMM, University of Montepellier, France, “Synchrotokens”, December, 2003.

ENST, Paris, France, “Adaptive System on a Chip for Low-Power Signal Processing”, December, 2003.

LIRMM, University of Montepellier, France, “Circuits for Long On-Chip Interconnects”, January 2003.

University of Bretagne Sud, L’Orient France, “Adaptive System on a Chip for Low-Power Signal Processing. May 2001 (part 2 in May 2002)

INSA Toulouse, France, “Current-Mode Circuits for Long Interconnect”. May 2001.

LIRMM, University of Montepellier, France, “Current-Mode Circuits for Long Interconnect”. May 2001. (part 2 in May 2002)

Intel, Circuits Research Lab, Hillsboro, Oregon, August 2001, “Current-Mode Circuits for Long Interconnects”.

Smith College, October 1999, “ Educational Innovations in Multimedia Systems”.
A similar presentation also made at the Asynchronous Learning Networks Conference in College Park, Maryland, November 1999 and to the UMass College of Engineering Dean’s Advisory Council, November 1999.

Alpha Development Group, Compaq Computer Corporation, June 1999, “ RLC Circuits for VLSI Designers” (a 6 hour short course).

Alpha Development Group, Compaq Computer Corporation, April 1999, “A Case for Current-Mode in Long Interconnects”.

Intel, Circuits Research Lab, Hillsboro, Oregon, June, 1998, “Circuits for Long Interconnects”.

ENST, Paris, FRANCE, May, 1998, “Reconfiguration for Power Savings in Real-time Motion Estimation”.

IRISA, Rennes, FRANCE, February, 1997, “Reconfigurable Communications Systems".

Motorola Research Center, Paris, FRANCE, April, 1997, “Reconfigurable Communications Systems".

IMEC, Leuven, BELGIUM, May 1997, “Reconfigurable Communications Systems".

Lecture tour in SOUTH KOREA, including Samsung Semiconductor, ETRI National Lab, Korean Advanced Institute of Science and Technology (KAIST), Pusan National University. “Advanced VLSI in Communications Systems", June, 1996. Funded by NSF, ETRI and Samsung.

Digital Semiconductor, Hudson, MA, “Low-Power CMOS VLSI Techniques", November, 1995

University of Utah, “VLSI Signal Processing: Systems Designs and CAD Tools", March 1995

Stanford University, “Wave-pipelining: A New Objective in High-Performance VLSI Design?", April 1994.

NEC, C.C. Research Labs, Princeton, New Jersey, “VLSI Signal Processing Research at UMass/Amherst", December 1994.

University of Colorado, “Coordinating VLSI Design, CAD Development and Communications Systems Design", October 1994.

Queens University, Belfast, Northern Ireland, “Using Regular Array Methods for DSP Module Synthesis", June 1994.

Ecole Nationale Superieure des Telecommunication (ENST), Paris, France. “Using Regular Array Methods for DSP Module Synthesis", May 1994.

Northeastern University, “ARREST: A Graphical Design Environment for VLSI Arrays", April 1993

University of Utah, “VLSI Research at UMass/Amherst", March 1992

Tufts University, “Structured VLSI Synthesis", February 1992

University of Colorado, “Structured VLSI Synthesis for DSP", October 1991

REFEREE/REVIEWER FOR:

National Science Foundation, (panels on CISE CAREER, EIA and Design Automation)
Swiss National Science Foundation
French National Science Foundation

IEEE Transactions on Circuits and Systems,
IEEE Transactions on Signal Processing,
IEEE Transactions on Computers,
IEEE Transactions on VLSI,
Journal of VLSI Signal Processing.
IEEE Signal Processing Magazine,
Computer Magazine,
Intl. Symposium on Circuits and Systems,
Intl. Conference on Computer Design,
Intl. Conference on Computer Aided Design,
Intl. Conference on Acoustics, Speech and Signal Processing,
Intl. Symposium on Low-Power Electronics and Design,
Design Automation Conference,
VLSI Design Conference,
VLSI Signal Processing Workshop (now Workshop on Signal Processing Systems),
Conference on Application-Specific Array Processors,
Great Lakes Symposium on VLSI.
Cryptographic Hardware and Embedded Systems

PUBLICATIONS

Below is a list of Books, Book Chapters, Refereed Conference papers and Journal papers. The total number of citations on Googlescholar as of June 2011 was approximately 3250 with h-index of 25.

BOOKS:

B1)*VLSI Signal Processing X*, T. Meng, K. Konstantinides, W. Burleson, IEEE Press. 1996. A collection of 40 leading papers on the design and implementation of signal processing systems.

B2) *Signal Processing Systems*, E. Manolakos, A. Chandrakasan, L.G. Chen, K. Konstantinides, W. Burleson, IEEE Press, 1998. A collection of 40 leading papers on the design and implementation of signal processing systems.

BOOK CHAPTERS:

BC1) R. Tessier and W. Burleson, "Reconfigurable Computing for Digital Signal Processing" in *Programmble Digital Signal Processors*, Marcel-Dekker (editor, Yu Hen Hu). 2001.

BC2) Mircea R. Stan, Wayne P. Burleson, "Bus-Invert Coding for Low-Power I/O", pp. 296-305, in *Low-power CMOS Design* edited by Anantha Chandrakasan, Robert Brodersen, IEEE Press, 1998.

JOURNALS:

Published or to appear:

J1) W. Burleson, L. Scharf, N. Endsley and A. Gabriel, "A Systolic VLSI Chip for Implementing Orthogonal Transforms", *Journal of Solid State Circuits*, Vol.24, No. 2, (April, 1989), pp. 466-468.

J2) W. Burleson, "Polynomial Evaluation in VLSI with Distributed Arithmetic", *IEEE Transactions on Circuits and Systems*, October, 1990, pp. 1299-1302.

J3) W. Burleson and L. Scharf, "A VLSI Design Methodology for Distributed Arithmetic", *Journal of VLSI Signal Processing*, 2 (1991), pp. 235-252.

J4) M. Stan, W. Burleson, C. Connolly, R. Grupen, "Analog VLSI for Robot Path Planning", *Journal of VLSI Signal Processing*, 8, 61-73 (1994).

J5) Y. Jeong, W. Burleson,"VLSI Array Synthesis for Polynomial GCD computation and Application to Finite Field Division", *IEEE Transaction on Circuits and Systems II*, December 1994, Vol 41,

J6) W.-H. Lien, W. Burleson,"Wave-Domino Logic: Theory and Application", *IEEE Transactions on Circuit and Systems II*, February, 1995, Vo. 42, No 2, pp 78-91.

J7) M. Stan, W. Burleson, "Bus-Invert Method for Low-Power I/O", *IEEE Transactions on VLSI Systems*, March, 1995, Vo. 3, No 1, pp 49-58.

J8) Y. Jeong and W. Burleson, "Array Algorithms and Architectures for RSA Modular Multiplication based on Precalculated Complements of the Modulus," *IEEE Transactions on VLSI Systems*, June 1997.

J9) M. Stan, W. Burleson "Low-Power Encodings for Global Communication in CMOS VLSI", *IEEE Transactions on VLSI Systems*, vol 5, no 4, Dec. 1997, pp. 444-455.

J10) B. Jung, W. Burleson, "VLSI Algorithm, Architecture and Implementation for High-Speed Lempel-Ziv Data Compression", *IEEE Transactions on VLSI Systems*, Sept 1998.

J11) B. Jung, W. Burleson, "Performance Optimization of Wireless Local Area Networks through VLSI Data Compression", *ACM Wireless Networks* Special Issue on VLSI in Wireless Networks, Winter 1998.

J12) W. Burleson, M. Ciesielski, F. Klass, W. Liu, "Wave-pipelining in VLSI: A Survey and Tutorial", *IEEE Transactions on VLSI Systems*, Sept, 1998.

J13) B. Jung, W. Burleson, "VLSI Architectures for Pyramid Vector Quantization", *Journal of VLSI Signal Processing Systems*, Winter 1998.

J14) W. Burleson, J. Ko, D. Niehaus, K. Ramamritham, J. Stankovic, G. Wallace, C. Weems "The Spring Scheduling Co-Processor: A Scheduling Accelerator" , *IEEE Transactions on VLSI*, November, 1998.

J15) R. Tessier and W. Burleson, "Reconfigurable Computing for Digital Signal Processing: A Survey", *Journal of VLSI Signal Processing Systems*, Fall 2000.

J16) W. Burleson, A. Ganz and I. Harris, "Educational Innovations in Multimedia Systems", *Journal of Engineering Education*, Winter 2000.

J17) A. Nalamalpu, S. Srinivasan, W. Burleson, "Boosters for Global Interconnect: Circuits, Design Methods and Comparison with Repeaters", *IEEE Transactions on Computer Aided Design*, Dec. 2001

J18) A. Maheshwari, W. Burleson and R. Tessier, "Trading-off Transient Fault-tolerance and Power Consumption in Deep Submicron (DSM) VLSI Circuits"**,** *IEEE Transactions on VLSI Systems*, volume 12, Issue 3, pp.299-311, March 2004.

J19) P. Jain,A. Laffely,W. Burleson,R. Tessier,and D. Goeckel,"Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations", *Journal of VLSI Signal Processing Systems*, vol 36, no. 1, pages 27-40, January 2004.

J21) A. Maheshwari, W. Burleson, "Differential Current Sensing for On-Chip Interconnects", *IEEE Transactions on VLSI Systems.* Volume 12, Issue 12, pp. 1321 – 1329, December 2004.

J20) J. Chittamuru, J. Euh and W. Burleson, "Power-Aware 3D Graphics Rendering", *Journal of VLSI Signal Processing Systems,* January, 2005.

J22) L. Bossuet, G. Gogniat, W. Burleson, "Dynamically Configurable Security for SRAM FPGA Bitstreams", *International Journal of Embedded Systems*. Issue 5/6 of 2005 .

J23) S. Swaminathan, R. Tessier, D. Goeckel, **W. Burleson**, "A Reconfigurable Viterbi Decoder in FPGAs", *IEEE Transactions on VLSI Systems.* Volume 13, Issue 4, pp.484 – 488, April 2005.

J24) M. Heath, **W. Burleson**, I. Harris, "Synchrotokens: A Deterministic GALS Methodology for Chip-Level Debug and Test", *IEEE Transactions on Computers*. Vol. 54, no. 12, December 2005.

J25) D. Jasinski, A. Maheshwari, A. Natarajan, W. Xu, R. Tessier, **W. Burleson**, "An Energy-Aware Active Smart Card, *IEEE Transactions on VLSI*., October 2005. (10 pages)

J26) Atul Maheshwari and **Wayne Burleson**, "Current-Sensing and Repeater Hybrid Circuit Technique for On-Chip Interconnects", *IEEE Transactions on VLSI*, November, 2007, (10 pages)

J27) Guy Gogniat, Tilman Wolf, **Wayne Burleson**, Jean-Philippe Diguet, Lilian Bossuet, and Romain Vaslin, "Reconfigurable hardware for high-security/high-performance embedded systems: The SAFES perspective", *IEEE Transactions on VLSI*, Volume 16, Number 2, February 2008. (10 pages)

J28) D. Holcomb, K. Fu, **W. Burleson** "Power-up SRAM State as an Identifying Fingerprint and Source of True Random Numbers", *IEEE Transactions on Computers*., December, 2009

J31) J. Zhao, S. Madduri, R. Vadlamani, **W. Burleson**, and R. Tessier, A Dedicated Monitoring Infrastructure For Multicore Processors, in *IEEE Transactions on VLSI Systems*, December 2010

J29) J. Jang, O. Franza, **W. Burleson** "Compact Expressions for Period Jitter in Binary Clock Trees", *IEEE Transactions on VLSI*, 2011.

J30) J. Zhao, S. Madduri, R. Vadlamani, **W. Burleson**, and R. Tessier, A Dedicated Monitoring Infrastructure For Multicore Processors, in IEEE Transactions on VLSI Systems, *IEEE Transactions on VLSI*, 2011.

J32) B.Datta, **W.Burleson** – Thermal Impact on Sub-Threshold Circuit Design, *Journal on Low-Power Electronics*, 2011.

JOURNALS Accepted but not yet in print

REFEREED CONFERENCES:

Published or to appear:

C1) W. Burleson and L. Scharf, "A VLSI Implementation of a Cellular Rotator Array", *Custom Integrated Circuit Conference* 1988, (4 pages).

C2) W. Burleson and L. Scharf, "VLSI Design of Inner Product Computers Using Distributed Arithmetic", *International Symposium on Circuits and Systems*, 1989, p. 158-161.

C3) W. Burleson and L. Scharf, "Input/Output Complexity of Bit-level VLSI Array Architectures", *Asilomar Conference on Signals, Systems and Computers*, Oct. 1989, (5 pages). (also presented at the *SIAM Conference on Parallel Processing for Scientific Computing*, Dec. 1989.)

C4) W. Burleson, "Memory Design for Bit-level VLSI Architectures", *Intl. Symposium on Circuits and Systems*, May, 1990, p. 2308-2311.

C5) W. Burleson, "VLSI Implementations of Census Computations: Meshes vs. Trees vs. Compromises", *Asilomar Conference on Signals, Systems and Computers*, Oct. 1990, p. 705-709.

C6) W. Burleson, "The Partitioning Problem on VLSI Arrays: I/O and Local Memory Complexity", *Intl. Conf. on Acoustics, Speech and Signal Processing,* 1991, p. 1217-1220.

C7) W. Burleson and L. Scharf, "Input/Output Design for VLSI Array Architectures", *International Conference on VLSI*, 1991, p. 357-366, (1 of 45 papers accepted out of 400 submitted).

C8) W. Marvin and W. Burleson, "A Simulator for General-Purpose Optical Array Architectures", *Intl. Conf. on Computer Design*, Cambridge, MA, October, 1991, p. 486-489.

C9) W.-H. Lien, W. Burleson, "Wave-Domino Logic: Theory and Application", *International Symposium on Circuit and Systems*, 1992, p. 2949-2952. (also presented at ACM/SIGDA *Workshop on Timing Issues in the Specification of Digital Systems,* 1992)

C10) Y.Jeong, W. Burleson, "Choosing VLSI Algorithms for Finite Field Arithmetic", *International Symposium on Circuit and Systems*, 1992, p. 799-802.

C11) W. Burleson, B. Jung, "ARREST: An Interactive Graphic Design Tool for VLSI Arrays", *International Conference on Application Specific Array Processors*, 1992, p. 149-162.

C12) M. Stan, W. Burleson, "Analog VLSI for Robot Path Planning", *Asilomar Conference on Signals, Systems and Computers*, 1992, p. 915-919.

C13) J. D. Narkiewicz, W. Burleson, "VLSI Performance/Precision Tradeoffs of Approximate Rank-Order Filters", *Workshop on VLSI Signal Processing*, p. 185-194.

C14) J. D. Narkiewicz, W. Burleson, "Rank-Order Filtering Algorithms: A Comparison of VLSI Implementations", *International Symposium on Circuits and Systems*, 1993. (4 pages)

C15) T. S. Kim, W. Burleson, M. Ciesielski "Logic Restructuring for Wave-pipelining", *International Workshop on Logic Synthesis*, 1993, (12 pages).

C16) W. Burleson, J. Ko, D. Niehaus, K. Ramamritham, J. Stankovic, G. Wallace, C. Weems, "The Spring Scheduling Coprocessor: A Scheduling Accelerator", *International Conference on Computer Design*, 1993, p. 140-144.

C17) H. Choi, W. Burleson, D.S. Phatak, "Optimal Wordlength Assignment for the Discrete Wavelet Transform in VLSI", *Workshop on VLSI Signal Processing*, 1993, p. 325-333.

C18) Y. Jeong, W. Burleson, "VLSI Array Synthesis for Polynomial GCD Computation" *International Conference on Application-Specific Array Processors*, 1993, p. 536-547, (1 of 19 full-length papers accepted out of 121 submitted).

C19) B. Jung, W. Burleson, "Node-Merging: A Transformation on Bit-level Dependency Graphs" *International Conference on Application-Specific Array Processors*, 1993, p. 442-453.

C20) Z. Zhou, W. Burleson, "Formal Descriptions, Semantics and Verification of VLSI Array Processors", *International Conference on Application-Specific Array Processors*, 1993, pp. 321-332.

C21) H. Choi, W. Burleson, D.S. Phatak, "Fixed-Point Roundoff Error Analysis of Large Feedforward Neural Nets", *International Joint Conference on Neural Networks*, 1993 (4 pages).

C22) W. Marvin, W. Burleson, D.S. Phatak, "Full Simulation of Optical Neural Nets", *Proc. of SPIE Conference on Neural Networks*, 1993, (13 pages).

C23) D. Niehaus, K. Ramamritham, J. Stankovic, G. Wallace, C. Weems, W. Burleson, J. Ko, "The Spring Scheduling Coprocessor: Design, Use and Performance", *Proceedings of the Real Time Systems Symposium*, 1993, (17 pages).

C24) T. S. Kim, W. Burleson, and M. Ciesielski,"Delay buffer insertion for Wave-pipelined Circuits", *International IFIP Workshop on Logic and Architecture Synthesis*, France 1993, (14 pages).

C25) W. Burleson, "Using Regular Array Methods for DSP Module Synthesis", *Hawaii International Conference on System Sciences*, 1994, p. I-58-67 (an invited session).

C26) B. Jung and W. Burleson, "A VLSI Systolic Array Architecture for Lempel-Ziv-based Data Compression" *International Symposium on Circuits and Systems*, 1994.

C27) M. Stan and W. Burleson "Limited-weight codes for low-power I/O", *International Workshop on Low-Power Design*, 1994.

C28) B. Jung, Y. Jeong and W. Burleson, "Distributed Control Synthesis for Data-Dependent Iterative Algorithms", *Conference on Application-Specific Array Processors*, 1994.

C29) W. Burleson, C. Lee and E. Tan, "A 150 Mhz Wave-pipelined Adaptive Digital Filter in 2 micron CMOS" *VLSI Signal Processing Workshop*, 1994.

C30) H. Choi and W. Burleson, "Search-based Wordlength Optimization in VLSI/DSP Synthesis" *VLSI Signal Processing Workshop*, 1994.

C31) W. Burleson, M. Ciesielski, W. Cotten and F. Klass, “Is Wavepipelining Practical?”, (A forum session), *Proceedings of International Symposium on Circuits and Systems*, 1994.

C32) B. Jung, W. Burleson, “Real-Time VLSI Compression for Wireless Local Area Networks", *Data Compression Conference*, 1995. p 431.

C33) Y. Jeong, W. Burleson, “High-level Estimation of High-Performance Architectures for Reed-Solomon Decoding", *International Symposium on Circuits and Systems*, 1995. pp. I-720-723.

C34) M. Stan and W. Burleson, “Coding a terminated bus for Low-power" *Great Lakes Symposium on VLSI*, 1995.

C35) Z. Zhou , W. Burleson, “Equivalence Checking of Datapaths based on Canonical Arithmetic Expressions”, *Design Automation Conference*, San Francisco, 1995.

C36) R. Grupen, C. Connolly, K. Souccar, and W. Burleson, "Toward a Path Co-Processor for Automated Vehicle Control," *IEEE Symposium on Intelligent Vehicles*, 1995.

C37) T. Kim, W. Burleson and M. Ciesielski, “Constrained Timing Synthesis and Delay insertion with Application to Wave-pipelining ", *ACM Workshop on Timing in Digital Systems*, 1995.

C38) M. Stan, and W. Burleson, “Low-Power CMOS Clock Drivers” *ACM Workshop on Timing in Digital Systems*, 1995.

C39) M. Stan, Wayne P. Burleson, “Synchronous Up/Down Counter with Period Independent of Counter Size”, *FPGA Conference*, 1996.

C40) M. Stan, and W. Burleson, “Two-dimensional Codes for Low-Power" *International Symposium on on Low-Power Electronics and Design*, 1996.

C41) W. Burleson, “Integrating Manufacturing into a Computer Systems Design Course: Design Technology and Industrial Collaboration", *IEEE Frontiers in Education Conference*, 1996.

C42) B. Jung and W. Burleson, “VLSI Array Architectures for Pyramid Vector Quantization", *VLSI Signal Processing Workshop* 1996.

C43) W. Burleson and M. Ciesielski, “Using Computers to Design Computers: Novel Instructional Technology in Computer Systems Engineering", *UMASS Instructional Technology Conference*, 1997.

C44) M. Petronino, W. Burleson, J. Carswell, J. Mead, R. Bambha, “FPGA-based Data Acquisition for 95Ghz Polarimetic Radar”, *International Conference on Acoustics, Speech and Signal Processing*, 1997.

C45) A. Brahmbhatt, W. Burleson, “FPGA-based Co-processors for Wireless Data Communications", *Massachusetts Telecommunications Conference*, 1997.

C46) S. R. Park, W. Burleson, “Frame-Rate Hardware Reconfiguration for Power Saving in Real-time Motion Estimation", *International Conference on Acoustics, Speech and Signal Processing*, 1998.

C47) S. R. Park and W. Burleson, “Configuration Cloning: Exploiting Regularity in Dynamic DSP Architectures”, *FPGA Conference*, 1999.

C48) W. Burleson, A. Ganz, I. Harris, “Multimedia Systems: An Integrated Modular Curriculum”, *University of Massachusetts Instructional Technology Conference* 1999.

C49) A. Garcia, W. Burleson, J.L. Danger, "Etude sur la consommation de puissance d'un dicodeur MPEG2 ` base des FPGA", *Journees D'Etude Faible Tension, Faible Consomma*tion, Paris, France. 1998, (in French).

C50) A. Garcia, W. Burleson, J.L. Danger, "Modele de la consommation de puissancedes FPGA". *Journees D'Etude Faible Tension, Faible Consomma*tion, Paris, France. 1998, (in French).

C51) A. Garcia, W. Burleson, J.L. Danger, "Power Modelling in FPGAs", *International Conference on Field Programmable Logic and Applications*, 1999.

C52) W. Burleson, A. Ganz, I. Harris, "Educational Innovations in Multimedia Systems", *Frontiers in Education Conference*, 1999. (Winner of Ben Dasher Award for Best Paper at entire conference.)

C53) A. Garcia, W. Burleson, J. Danger "Low Power Digital Design in FPGAs: A Study of Pipeline Architectures Implemented in a FPGA Using a Low Supply Voltage to Reduce Power Consumption", *FPGA Conference*, 2000. Updated version presented at *ISCAS*, 2000.

C54) J. Peden, C. Leonardo, W. Burleson, "The Multimedia Online Collaboration Architecture, *UMass Instructional Technology Conference*, 2000.

C55) R. Adrion, J. Kurose, W. Burleson, et al , "Multimedia Asynchronous Networked Information Courseware", *UMass Instructional Technology Conference*, 2000.

C56) W. Burleson, J. Peden, C. Leonardo, "Distributed VLSI Design with the Multimedia Online Collaboration Architecture", *European Workshop on Microelectronics Education*, May 2000

C57) A. Nalamalpu and W. Burleson, "Repeater Design in DSM CMOS: Novel Analytical Model and Placement Sensitivity Analysis", *International Symposium on Circuits and Systems,* 2000.

C58) J. Peden, W. Burleson, C. Leonardo, "The Multimedia Online Collaboration Architecture: Tools to Enable Distance Learning" *International Conference on Multimedia and Exposition*, Aug, 2000.

C59) J. Euh, W. Burleson, "Exploiting Content Variation and Perception in Power-Aware 3D Graphics Rendering". *Workshop on Power-Aware Computing*, Fall 2000.

C59) W. Burleson, P. Jain, S. Venkatraman, "Dynamically Parameterized Architectures for Power-Aware Video Coding: Motion Estimation and DCT*", IEEE Workshop on Digital and Computational Video*, 2001

C60) W. Burleson, R. Tessier, D. Goeckel, P. Jain, A. Laffely, "Dynamically Parameterized Algorithms and Architectures for Low-Power Signal Processing, *International Conference on Acoustics Speech and Signal Processing*, 2001

C61) A. Maheshwari and W. Burleson, "Current-sensing for Global Interconnects, Secondary Design Issues: Analysis and Solutions". *IEEE International Workshop on Power and Timing* M*odeling, Optimization and Simulation*. Sept, 2001

C62) S. Thampuran, K. Watts, W. Burleson, "CD-MANIC: Multimedia Distance Education without the Wait", *IEEE Frontiers in Education*, 2001.

C63) A. Nalamalpu, W. Burleson, "Booster Circuits for Long CMOS Interconnects", *IEEE Symposium on Physical Design*, April 2001.

C64) M. Sinha, W. Burleson, "Current-sensing for Crossbars", *IEEE ASIC/SOC conference*, 2001.

C65) A. Nalamalpu, W. Burleson, "Repeater Insertion in Deep Submicron CMOS: Practical Issues for Area and Power Minimization", *IEEE ASIC/SOC Conference*, 2001

C66) A. Laffely, W. Burleson, R. Tessier, J. Liang, "Adaptive System on a Chip for Low-Power Signal Processing", *Asilomar Conference on Signal and Systems*, October 2001.

C67) A. Maheshwari, W. Burleson, R. Tessier, "Trading Off Power and Reliability in Ultra-Low Power Systems", *IEEE International Symposium on Quality in Electronic Design*, March 2002.

C68) S. Swaminathan, R. Tessier, D. Goeckel, W. Burleson, "An Adaptive Viterbi Decoder in FPGAs", *FPGA Conference*, 2002.

C69) A. Maheshwari, S. Srinivasaraghavan, W. Burleson, "Quantifying the Impact of Current-Sensing on Interconnect Delay Trends", *IEEE ASIC/SOC Conference,* 2002.

C70) J. Chittamuru, J. Euh, and W. Burleson, "An Adaptive Low Power Texture Mapping Architecture", *IEEE Mid-West Symposium On Circuits and Systems*, 2002 pp. 204-208.

C71) J. Euh, J. Chittamuru, and W. Burleson, "CORDIC Vector Interpolator for Power-Aware 3D Computer Graphics", *IEEE Workshop on Signal Processing Systems*, 2002, 426-431.

C72) W. Burleson, S. Kelley, S. Thampuran "A New Course in Multimedia Systems for Non-Technical Majors", *ASEE Engineering Education Conference and Exposition*, June, 2002. pp 2793-2802.

C73) W. Burleson, W. Cooper, J. Kurose, S. Thampuran, K. Watts, "An Empirical Study of Student Interaction with CD-based Multimedia Courseware", *ASEE Engineering Education Conference and Exposition*, June, 2002. pp 1430-1443.

C75) W. Burleson, S. Thampuran N. Ramaswamy, "Multimedia Systems: Enabling Computer Engineering Education", *IEEE Frontiers in Education Conference*, 2002.

C76) J. Chittamuru, and W. Burleson, "Dynamic Wordlength Variation for Low-Power 3D Graphics Texture Mapping", *IEEE Workshop on Signal Processing Systems*, 2003.

C77) M. Sinha, S. Hsu, A. Alvandpour, W. Burleson, R. Krishnamurthy, S. Borkar, "High-Performance and Low Voltage Sense-Amplifier Techniques for Sub-90nm Caches", *IEEE ASIC/SOC Conference,* 2003.

C78) M. Sinha, S. Hsu, A. Alvandpour, W. Burleson, R. Krishnamurthy, S. Borkar, "Low Voltage Sensing Techniques and Secondary Design Issues for Sub-90nm Caches", *European Solid State Circuits Conference,* 2003.

C78) S. Srinivasaraghavan, W. Burleson, "Interconnect Effort: A Unification of Repeater Insertion and Logical Effort", *IEEE International Symposium on VLSI*, 2003.

C79) A. Laffely and W. Burleson, "Using System on a Chip for VLSI Education", *IEEE Microelectronic Systems Education Conference*, June 2003.

C80) A. Laffely, J. Liang, W. Burleson, R. Tessier "Adaptive System on a Chip: A Backbone for Power-Aware Signal Processing Cores", *IEEE International Conference on Image Processing*, September 2003.

C81) A. Natarajan, D. Jasinski, W. Burleson, R. Tessier, "A Hybrid Adiabatic Content Addressable Memory for Ultra-Low Power Applications", *ACM Great Lakes Symposium on VLSI*, 2003.

C82) A. Maheshwari and W. Burleson, "Repeater and Current-sensing Hybrid Circuits for On-chip Interconnects" , *ACM Great Lakes Symposium on VLSI,* 2003.

C83) V. Venkatraman, A. Maheshwari , W. Burleson, **"**Mitigating Static-Power in Current-Sensed Interconnects", *ACM Great Lakes Symposium on VLSI,* 2004.

C84) V. Venkatraman, A. Laffely, J. Jang, Z. Zhu, H. Kukkamalla, W. Burleson, **"**NoCIC: A Spice-based Interconnect Planning Tool Emphasizing Aggressive On-Chip Interconnect Circuit Methods**,** *International Workshop on System Level Interconnect Prediction,* 2004.

C85) M. Heath, W. Burleson and I. Harris, "A Deterministic Globally Asynchronous Locally Synchronous (GALS) Methodology for Validation, Debug, and Test", *Design Automation and Test in Europe*, 2004

C86) L. Bossuet, G. Gogniat, W. Burleson, "Dynamically Configurable Security for SRAM FPGA Bitstreams", *Reconfigurable Architectures Workshop*, 2004

C87) A. Maheshwari, I. Koren, W. Burleson , "Accurate Estimation of Soft Error Rates (SER) in VLSI Circuits", *IEEE Conference on Defect and Fault-tolerance in VLSI*, 2004.

C88) V. Venkatraman, W. Burleson, "Impact of Process Variation on Multi-level Signaling for On-Chip Interconnects", *International Conference on VLSI Design*, 2005.

C89) N. Salzmann, W. Burleson, K. Rubin, K. Kloesel, S. Cruz-Pol, O. El-Hakim, "Challenges in a Multidisciplinary K12 Summer Content Insitute", *ASEE* 2005.

C90) O. Hoffman, T. Djaferis, P. Dobosh, W. Burleson, "Moving towards a more Systems Approach in a Robotics based Introductory Engineering Course at Mt. Holyoke College", *ASEE* 2005.

C91) S. Hsu, V. Venkatraman, S. Mathew, H. Kaul, M., S. Dighe, W. Burleson, R. Krishnamurthy, "A 2GHz 13.6mW 12x9b Multiplier for Energy Efficient FFT Accelerators**",** *Proc. of the 31st European Solid-State Circuits Conference,* Sep. 2005 .

C92) V. Venkatraman and W. Burleson, "Robust Multi-Level Current-Mode On-Chip Interconnect Signaling in the Presence of Process Variations**",** *Sixth International Symposium on Quality of Electronic Design, March 2005, pp: 522-527*

C93) J. Jang, S. Xu, W. Burleson, "Jitter in Deep Sub-micron Interconnect"**,** *IEEE Computer Society Annual Symposium on VLSI,* 2005.

C94) A. Natarajan, V. Shankar, A.Maheshwari, W. Burleson, "Sensing Design Issues in Deep Submicron CMOS SRAMs"**,** *IEEE Computer Society Annual Symposium on VLSI,* 2005.

C95) W. Burleson, T. Wolf, R. Tessier, W. Gong, G. Gogniat, "Embedded System Security: A Configurable Approach", *International Conference on Homeland Security*, 2005.

C96) G. Gogniat, L. Bossuet, and W. Burleson, **"**Configurable computing for high-security/high-performance ambient systems", *Embedded Computer Systems: Architectures, MOdeling, and Simulation (SAMOS V)* July, 2005.

C97) B. Wallace, W. Richards Adrion, W. Burleson, W. Cooper, J. Cori and K. Watts, "Using Multimedia to Support Research, Education and Outreach in an NSF Engineering Research Center", *Frontiers in Education (FIE),* 2005.

C98) W. Burleson and S. Xu, "Digital Systems Design with ASIC and FPGA: A Novel Course using CD/DVD and On-line Formats"**,** *International Conference on Microelectronic Systems Education,* 2005.

C99) G. Gogniat, T. Wolf, and W. Burleson, Reconfigurable Security Primitive for Embedded Systems, *IEEE International Symposium on System-on-Chip (SOC 2005)*
November, 2005.

C100) G. Gogniat, T. Wolf, and W. Burleson, Reconfigurable Security Architecture for Embedded Systems, to appear at the *Mobile Computing Hardware Architectures: Design and Implementation Design Symposium (MOCHA 2006),* January, 2006.

C101) I. Benito, V. Venkatraman, W. Burleson, Process Variation-Aware Vdd Assignment Technique for Repeated Interconnects, *49th IEEE International Midwest Symposium on Circuits and Systems*, 2006.
pdf-link (219.3kB)

C102) S. Xu, V. Venkatraman and W. Burleson, Energy-Aware Differential Current Sensing for Global On-Chip Interconnects, *49th IEEE International Midwest Symposium on Circuits and Systems*, 2006. pdf-link (197kB)

C103) Tilman Wolf, Shufu Mao, Dhruv Kumar, Basab Datta, Wayne Burleson, and Guy Gogniat. "Collaborative monitors for embedded system security". In Proc. of First International Workshop on Embedded Systems Security in conjunction with 6th Annual ACM International Conference on Embedded Software (EMSOFT), Seoul, Korea, October 2006.

C104) V. Venkatramn, M. Anders, H. Kaul, **W. Burleson**, R. Krishnamurthy "A low-swing signaling circuit technique for 65nm on-chip interconnects" IEEE International SOC Conference, Sept. 2006: 289-292.

C105) V. Ambrose, W. Burleson, D. Holcomb, S. Mukherjee, J. Pickholtz, "A Fast and Accurate Method for Simulating Soft Errors in Large Combinational Circuits", Intel Design and Test Technology Conf., 2007.

C106) Daniel E. Holcomb, Wayne P. Burleson, and Kevin Fu. Initial SRAM state as a fingerprint and source of true random numbers for RFID tags. In Proceedings of the Conference on RFID Security, July 2007.

C107) S. Xu, I. Benito, W. Burleson: Thermal Impacts on NoC Interconnects. IEEE NOCS 2007 (6 pages)

C108) R. Vaslin, G. Gogniat, J.-P. Diguet, E. Wanderley, R. Tessier and **W. Burleson**, Low Latency Solution for Confidentiality and Integrity Checking in Embedded Systems with Off-Chip Memory, in the Proceedings of the International Conference on Reconfigurable Communication-centric SoCs, Montpellier, France, June 2007.

C109) R. Vaslin, G. Gogniat, J.-P. Diguet, **W. Burleson**, and R. Tessier, High-Efficiency Protection Solution for Off-Chip Memory in Embedded Systems, in the Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms, Las Vegas, NV, June 2007.

C110) D. Kumar and **W. Burleson**, "Distributed Collaborative Adaptive Sensing: A Unifying Theme for a Junior Level Embedded Systems Course", IEEE Microelectronics Systems Education Conference, 2007 (2 pages).

C111) B.Datta, **W.Burleson** – Low Power and Robust On-Chip Thermal Sensing using Differential Ring Oscillators, IEEE Mid-west Symposium on Circuits and Systems, July 2007.

C112) B.Datta, **W.Burleson** – ThermoWire: A Fast, Robust, low-power Interconnect based thermal sensor, IEEE VLSI-SoC October, 2007.

C113) V. Venkatraman and **W. Burleson**, "An Energy-efficient Multi-bit Quaternary Current-mode Signaling for On-chip Interconnects", IEEE Custom Integrated Circuits Conference (CICC), Sept 2007

C114) B. Datta, **W. Burleson** " Collaborative Sensing of On-Chip Wire Temperatures using Interconnect based Ring Oscillators", IEEE Great Lakes Symposium on VLSI, 2008

C115) V. Arunachalam, **W. Burleson**, "Low-Power Clock Distribution in a Multilayer Core 3D Microprocessor ", IEEE Great Lakes Symposium on VLSI, 2008

C116) L. Lin, **W. Burleson**, "Leakage-Based Differential Power Analysis (LDPA) on Sub-90nm CMOS Cryptosystems", IEEE ISCAS 2008

C117) J. Jang, O. Franza (Intel), **W. Burleson**, "Period Jitter in Global Clock Trees", IEEE Workshop on Signal Propagation on Interconnects (SPI), 2008.

C 118) Jinwook Jang Franza, O. Burleson, W. , Compact expressions for period jitter of global binary clock trees, Electrical Performance of Electronic Packaging, 2008 IEEE-EPEP.

C119) B.Datta, W.Burleson – Temperature Measurement in Content Addressable Memory Cells using Bias Controlled VCO, IEEE International System-On-Chip Conference (SOCC), October 2008, Newport Beach

C120) B.Datta, W.Burleson – On Temperature Planarization effect of Copper Dummy Fills in Deep Nanometer Technology, IEEE International Symposium on Quality Electronic Design (ISQED), 2009, San Jose

C121) B.Datta, W.Burleson – Temperature Effects on Energy Optimization in Sub-Threshold Circuit Design, IEEE International Symposium on Quality Electronic Design (ISQED), 2009, San Jose

C122) B.Datta, W.Burleson, Low-Power, Process-Variation Tolerant On-Chip Thermal Monitoring using Track and Hold Based Thermal Sensors, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009, Boston

C123) B.Datta, W.Burleson – Temperature Effects and Thermal Sensing in Sub-Threshold, SRC TECHCON, 2009

C124) S. Madduri, R. Vadlamani, W. Burleson and R. Tessier, A Monitor Interconnect and Support Subsystem for Multicore Processors , DATE 2009.

C125) Lang Lin, Wayne Burleson. Analysis and Mitigation of Process Variation Impacts on Power-Attack Tolerance. In Proceedings of ACM/IEEE Design Automation Conference, July 2009.

C126) Lang Lin, Markus Kasper, Tim Guneysu, Christof Paar, Wayne Burleson. Trojan side-channels: lightweight hardware Trojans through side-channel engineering. In Workshop on Cryptographic Hardware and Embedded Systems (CHES), September 2009.

C127) Lang Lin, W. Burleson, C. Paar, "MOLES: Malicious Off-Chip Leakage Enabled by Side-Channels", ICCAD 2009.

C128) C. Paar, A. Rupp, K. Schramm, A. Weimerskirch, W. Burleson, Securing Green Car: IT Security in Next-Generation Electric Vehcile Systems,, Annual Meeting and Exposition of the Intelligent Transportation Society of America, 2009.

C129) B.Datta, W.Burleson – Circuit-level NBTI Macro-Models for Collaborative Reliability Monitoring, ACM Great Lakes Symposium on VLSI (GLSVLSI), Providence, 2010

C130) B Datta, W Burleson, Calibration of on-chip thermal sensors using process monitoring circuits", ISQED, 2010

C131) B Datta, W Burleson, "Analysis and mitigation of NBTI-impact on PVT variability in repeated global interconnect performance" - GLSVLSI 2010

C132) J Zhao, B Datta, W Burleson, R Tessier , "Thermal-aware voltage droop compensation for multi-core architectures", GLSVLSI 2010.

C133) R Vadlamani, J Zhao, W Burleson, R. Tessier "Multicore Soft Error Rate Stabilization Using Adaptive Dual Modular Redundancy" DATE 2010

C134) Low-Power Sub-threshold Design of Secure Physical Unclonable Functions.
by L. Lin, D. Holcomb, D. K. Krishnappa, P. Shabadi, W. Burleson.
ISLPED, August 2010. An earlier version appear at the Workshop on Secure Component and System Identification SECSI, Cologne, Germany, April 2010.

C135) VB Suresh, WP Burleson "Entropy extraction in metastability-based TRNG", International Symposium on Hardware-Oriented Security and Trust (HOST) 2010

C136) J. Jang, W. Burleson, **An arbiter based on-chip droop detector system**, *ACM Great Lakes Symposium on VLSI (GLSVLSI), 2011*. acm

C137) V. Suresh, W. Burleson, **A Hybrid Self-calibration Technique to Mitigate the Effect of Variability in TRNG**, *2nd European Workshop on Variability, VARI 2011*. pdf

C138) B.Datta, W.Burleson, **A Tunable Glitch Filtering Circuit Using Variable Threshold Inverters**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio De Janeiro, 2011. pdf

C139) B.Datta, W.Burleson, **A High Sensitivity and Process Tolerant Thermal Sensing Scheme for Liquid Cooled 3-D ICs**, *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Lausanne, 2011. pdf

C140) B.Datta, W.Burleson, **A 45.6u^2 13.4uW 7.1V/V Resolution Sub-Threshold Based Digital Process Sensor in 45nm CMOS**, *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Lausanne, 2011. pdf

C141) B.Datta, W.Burleson, **A 12.4um^2 133.4uW 4.56mV/ºC Resolution Digital On-Chip Thermal Sensor in 45nm CMOS Utilizing Sub-Threshold Operation**, *IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, 2011. pdf

C142) G.T. Becker, W. Burleson, C. Paar, Side-channel Watermarks for Embedded Software, *9th IEEE NEWCAS Conference*, June 2011. pdf

C143) K. Chillara, J. Jang, W. Burleson, **Robust Signaling Techniques for Through Silicon Via Bundles,** *ACM Great Lakes Symposium (GLSVLSI)*, 2011. pdf

C144) S.K.Srivathsaand W.Burleson, "**Subthreshold design of physical unclonable functions**", *IEEE Subthreshold Microelectronics Conference* , 2011.

BOOK REVIEWS:

1) W. Burleson, "Digital Signal Processing - Theory, Hardware and Applications" by Haddad and Parsons, in *Computer Magazine*, October, 1992.

2) W. Burleson, "Anatomy of a Silicon Compiler" by R.W. Brodersen, *Computer Magazine*, July 1994, p. 117.

PATENTS

1. United States. Patent 4,626,825 A Logarithmic Conversion Apparatus

2. United States Patent 4,862,346 Index for a register file with update of addresses using simultaneously received current, change, test, and reload addresses

3 United States Patent 5,109,524 Digital processor with a four port data register for storing data before and after data conversion and data calculations

4. United States Patent 7,279,939 Circuit for differential current sensing with reduced static power

5.. United States Patent Application 20070250755, Dormant error checker,

6.. United States Patent 7,529,118, "Generalized Interlocked Cell,",