A High Sensitivity and Process Tolerant Digital Thermal Sensing Scheme for 3-D ICs

Basab Datta
Electrical and Computer Engineering Department
University of Massachusetts-Amherst
bdatta@ecs.umass.edu

Wayne Burleson
Electrical and Computer Engineering Department
University of Massachusetts-Amherst
burleson@ecs.umass.edu

ABSTRACT
Thermal sensing is a pressing need in stacked 3-D chips with limited number of vertical heat conduits. In 3-D systems with active temperature control, the controller is reliant on sensors placed on individual planes to provide the necessary thermal feedback. To this end we propose a delay-line based thermal-sensor which provides a high temperature-sensitivity, high level of process-robustness and is amenable to the TSV-based communication paradigm used in 3D systems. The temperature-sensitive piece mitigates the high process-susceptibility of 3-D circuits through usage of multiple logic-stages composed of long-channel devices and elimination of common-mode noise on the delay-line pair. The thermal information is conveyed to the controller in the form of a signal-frequency and hence is insensitive to path-mismatch in TSV wires. A high post-digitization temperature sensitivity of 0.82%/°C was achieved. The 1-σ accuracy loss due to process-variations and supply-noise was limited to 0.78°C and 1.06°C respectively indicating a high level of process-tolerance.

Categories and Subject Descriptors
B.7 [Integrated Circuits]: Types and Design Styles

General Terms
Measurement, Design

Keywords
3-D, thermal-sensor, delay-line, process-variation, TSV

1. INTRODUCTION
The aggressive scaling of device dimensions has enabled a continuous increase in clock-rates and functionality by virtue of reduction in gate-delays [1]. However, current technology scaling trends have caused the interconnect delays to increase progressively with every generation making interconnect performance the dominant and limiting factor in chip performance and power-consumption [2]. Vertical integration of logic planes, also known as a stacked 3-D IC, has emerged as a compelling solution to overcome the performance bottleneck presented by interconnects. 3D stacking has been proven to significantly reduce both the number as well as length of long nets [3]. This reduction in length of wire-nets is readily translated into a significant reduction in interconnect delays and power dissipation [4].

A fundamental challenge in the design of 3-D circuits is joule heating. While absolute power consumption decreases due to reduction in interconnect length, the increase in device density due to multiple logic planes stacked over the same area causes the power-density to increase drastically. The high power-density coupled with the low thermal conductivity of the Inter-Layer-Dielectrics (ILD) significantly exacerbates the thermal problem in 3-D ICs [5] [6]. High temperatures on the planes far from the heat-sink results in degraded performance and accelerated wear-out mechanisms. Thus, exploiting the performance benefits of vertical integration while simultaneously containing thermal effects is a topic of extensive research in 3-D ICs.

Research on circuit-cooling schemes for 3-D ICs can be broadly classified into 2 categories: heat-sink based methods and internal heat distribution based methods [5]. In conventional 2-D microprocessors, cooling is performed by attaching a heat-sink to the package and removing the heat from the sink using fans [1]. In 3D, the poor thermal conductivity of the ILD layers inhibit the device heat from being effectively dissipated towards the heat-sink rendering heat-sink based methods largely ineffective [7][8]. The thermal problem can be tackled at the design stage itself using static or dynamic methods. A static optimization technique is to add temperature as an optimization objective during 3-D floor-planning [9] or placement [10]. Significant research effort has been expended towards modeling and utilizing the heat-removal characteristics of Through Silicon Vias (TSV) through controlled grid-like or non-uniform placement of TSVs [5][11-13]. Among dynamic temperature control mechanisms, liquid cooling has emerged as a compelling candidate for heat-removal in 3-D chips. It is performed by attaching a cold-plate with built-in micro-channels or fabricating micro-channels between the layers [7]. A coolant fluid is then pumped through the micro-channels to enable heat-exchange [1]. Precise flow-rate control for each plane is necessary since pessimistic cooling might degrade reliability and cooling efficiency while an optimistic flow-rate might cause an unwanted increase in temperature dependent leakage power offsetting the power-benefits of cooling [7] [14]. 3-D systems with DTM capability allocate the workload or adjust the coolant flow rate based on the thermal status of individual planes. Thus, performance of a dynamic thermal management unit in 3-D ICs strongly depends upon the accuracy of the temperature information obtained from each core in a 3-D stack.

In this paper, we propose a high-sensitivity and process-tolerant thermal-sensing scheme which can be used to convey the thermal information from individual planes to the controller plane. We present a delay-line based thermal sensor having a high post-digitization sensitivity of 0.82%/°C. The design is particularly suitable for sensing in 3-D systems since it offers a high level of process-robustness. The 1-σ accuracy loss due to process-variations and supply-noise was found to be 0.78°C and 1.06°C respectively. We performed a latency analysis for TSV-based communication of thermal information and present a communication strategy based on sequential access of sensors using shared TSVs.

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2. TEMPERATURE MONITORING IN 3-D

2.1 Related Work

On-chip thermal sensors can be classified based on their output type: current, voltage, delay, frequency and leakage-decay period. Among voltage-output sensors, thermal diodes have remained the de facto industrial standard for 2-D sensing providing a reasonably high sensitivity of -1.6mV/ºC at the cost of a high area/power overhead [15]. Several frequency output thermal sensors have been proposed in literature making use of the temperature dependent parameters of MOS transistor/microelectronic structures present on an IC [16]. These however occupy a large silicon area, have a considerably high power-requirement and are significantly affected by process-variations rendering their usage as sensors unreliable in the sub-90nm regime. Leakage based thermal sensors have been proposed in [17] and [18]. Leakage is a highly process-dependent parameter and at higher temperatures the sensor-response curves become asymptotic making it difficult to discern consecutive measurements and compromising the accuracy of the sensor. Time-to-Digital conversion based thermal sensors [19][20] offer a high-level of robustness to process and supply-variations but suffer from a limited measurement range due to non-linearity of the output at the higher temperatures. For 3-D systems process-tolerance is an extremely important design requirement since they have both inter-die and intra-die variations in equal measure (as opposed to 2-D systems where within die variations dominate). Thus, we adopt a delay-line based sensing architecture for our design and propose a configuration of delay-elements which can offer a high resolution for the entire temperature-range of concern.

2.2 Thermal Monitoring Scheme in 3-D

In 3-D systems having the capability to perform active thermal control, its assumed that each core is equipped with a thermal-sensor and the temperature feedback is utilized to make job-scheduler decisions and adjust the coolant flow-rate. The controller uses the temperature feedback from individual planes and a variety of reactive/predictive algorithms to forecast the maximum system temperature. Based on the temperature predictions for the next time-steps, the controller proactively allocates the work-load to individual planes or adjusts the coolant flow-rate (as shown in Fig.1) Our goal was to devise a thermal sensing scheme that could fit into the DTM paradigm typically adopted by 3-D ICs.

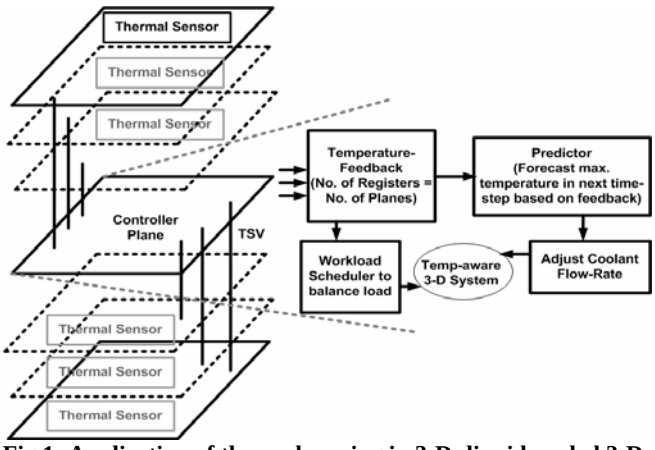

Fig 1: Application of thermal sensing in 3-D: liquid-cooled 3-D systems utilizing thermal feedback from individual planes [7]

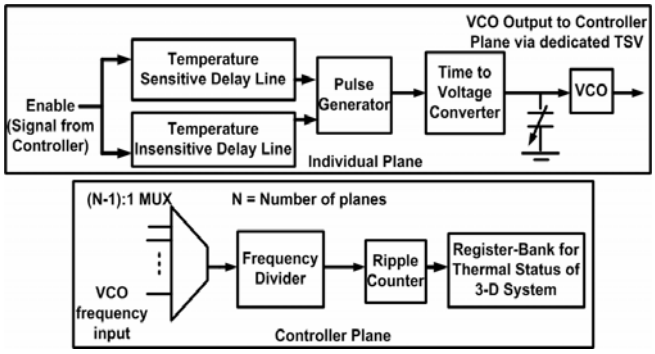

Fig 2: Block-level diagram of thermal-sensing system

A thermal-sensor for 3-D systems has 2 primary design requirements: 1) It should offer high sensitivity and at the same time be extremely robust towards process-variations 2) The sensing system should be amenable to the TSV-based communication paradigm employed in 3-D. To this end we propose a design with high temperature-sensitivity based on delay-lines. Fig.2 gives a block-level overview of the sensing system. A temperature-sensitive and a temperature-insensitive delay line are used in conjunction to generate a digital pulse whose width is proportional to the temperature of the temperature-sensitive circuit-piece. A Time-to-Voltage converter is used convert the pulse into a finite charge (analog) stored on a capacitor. After loop-filtering, the voltage across the capacitor is then used as the control voltage for a VCO. The VCO output serves as a proxy for the thermal-status of the particular plane and is transmitted via a TSV to the controller plane. The design is replicated on each plane in the 3-D system. On the controller plane, the VCO outputs from different planes are multiplexed and fed to a frequency divider followed by a ripple counter in order to digitize the thermal information. The sensed digital bit-stream could then be stored in a register-bank from where the controller could read out values periodically and run temperature prediction algorithms to decide on the optimum coolant flow-rate. The proposed design has the dual advantage of being process-tolerant due to usage of delay-lines for thermal-sensing and being relatively insensitive to path-mismatch in TSV wires due to usage of frequency as the output metric.

2.3 Design of Temperature Sensitive and Insensitive Delay Lines

In this section, we discuss the basic circuits needed to perform thermal-sensing on each plane. We propose a novel, tunable temperature sensitive delay-element which is capable of generating a sufficiently large delay variation per degree-Celsius rise in temperature. The delay-element is basically a tunable threshold buffer whose switching threshold varies with temperature (Fig.3(i)). It comprises of a series of transmission gates which act as low-pass filters to the input signal and also, offer a finite resistance to the signal path. The path resistance is directly proportional to the temperature of the delay-element. In the case of a low-to-high transition, the NMOS-devices are turned ON and a logic ‘1’ is passed while in the case of a high-to-low transition the PMOS-devices are turned ON and a logic ‘0’ is passed. The effective resistance is linearly proportional to the number of transmission gates in the path. For CMOS circuits operating at a high supply-voltage (1.0V in 45nm), the mobility-effect dominates in determining the behavior of the circuit under thermal stress. With rise in temperature, the effective path-

resistance across the active chain of transmission-gates increases and it causes the switching-threshold of the inverter to shift farther away from its nominal point. Thus, a signal-delay with a high sensitivity to temperature is generated by the delay-element.

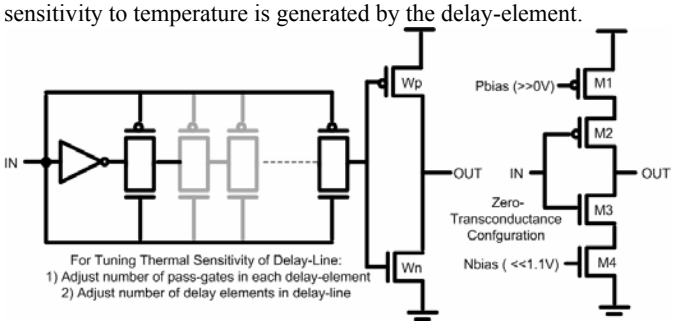

Fig 3: (i) Temperature sensitive (TS) delay-element (ii) Temperature-insensitive (TI) delay-element

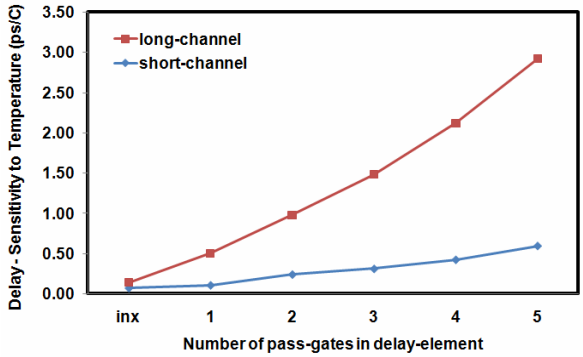

Fig.4 Delay-sensitivity variation with number of pass-gates

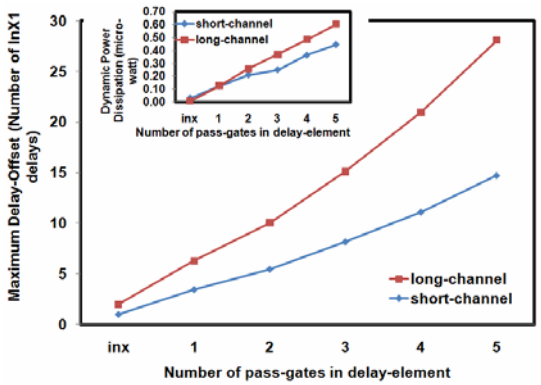

Fig.5 Delay-offset and power overhead of temperature-sensitive delay-element for varying number of pass-gates

Unlike traditional thermal sensors where only the relative temperature-sensitivity of the sensor-output matters, in the case of delay-line based thermal-sensing, the absolute delay-variation with temperature is just as important since it directly affects the resolution of the sensor. The design goal was to ensure a sufficiently large delay-variation with temperature while at the same time minimizing the delay-offset (delay across the element at 25°C). A large delay-offset is detrimental towards the design since it would require a delay of similar magnitude to be generated by the temperature-insensitive delay-line which in turn will increase the area and power overhead. Using 65nm PTM models [22], we found the delay-sensitivity to temperature to increase linearly with the number of pass-gates in the delay-element (Fig.4). The long-channel devices were found to offer a significantly higher delay-sensitivity for multiple transmission-gates in the delay-element and on the flip-side, a higher delay-offset. There exists a trade-off between the delay-sensitivity to temperature and the granularity of delay-offset achieved by a single delay-element. Using a large number of gates resulted in significantly higher delay-offset and dynamic power dissipation (Fig.5). Thus, in our design we restricted ourselves to only 2 transmission gates per delay-element. The desired magnitude of delay-variation with temperature (~7ps/°C) was achieved by cascading 5 delay-elements; each one composed of two transmission-gates designed with long-channel devices.

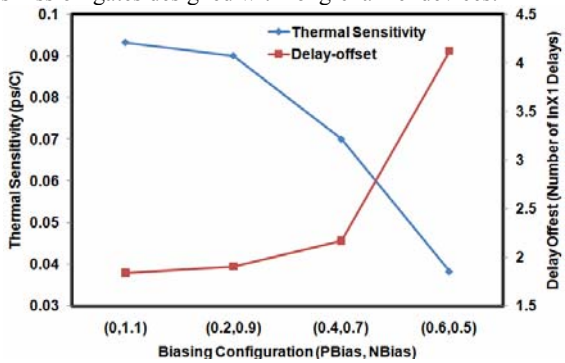

Fig.6 Sensitivity variation Vs delay-offset for different biasing configurations of temperature-insensitive delay-element

For the temperature-insensitive delay-line we used a current-starved inverter as the main delay-element (Fig.3(ii)). Temperature invariance was achieved by varying the biasing applied to the current-starving devices till Zero-Temperature-Coefficient (ZTC) point was achieved for transistors M2 and M3. The design goal for this delay-line was to simultaneously achieve temperature invariance and match the delay-offset of the temperature-sensitive delay-line. A favorable aspect of this particular design choice was that the biasing configuration providing the least temperature sensitivity also provided the maximum delay-offset (PBias=0.6V, NBias=0.5V) which minimized the number of such delay-elements required (Fig 6).

2.4 Pulse-Width Generation

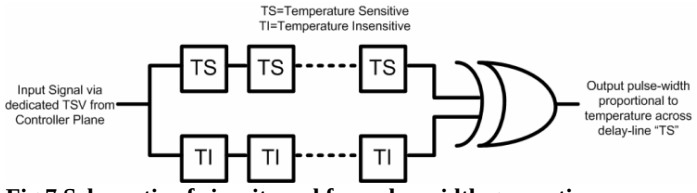

Fig.7 Schematic of circuit used for pulse-width generation

The circuit used for generation of temperature-dependent pulses is similar to the one proposed in [19] (Fig.7). Both the temperature-sensitive and the temperature-insensitive delay lines were configured in such a way that a minimum number of delay-elements were used and a close matching was achieved between the 2 delay-lines at the nominal temperature of 25°C. The XOR output remained 'high' as long as either of the 2 delay-line outputs was 'high'. In our design, the temperature-insensitive delay-line was faster while delay across the temperature-sensitive delay-line increased progressively with rise in temperature causing the output pulse-width to increase linearly with temperature (Fig.8). A high resolution of 6.23ps/ °C was achieved which translated into a high temperature-sensitivity of 2.03%/ °C.

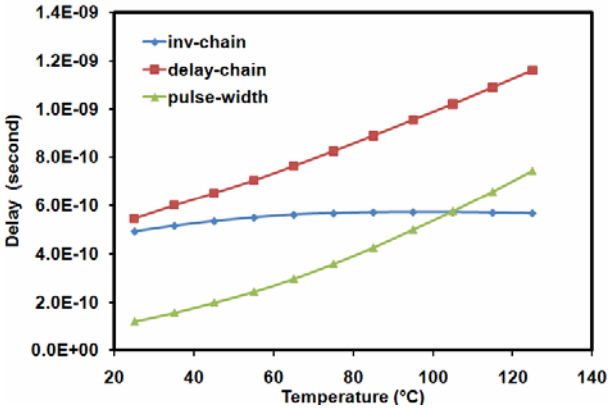

Fig.8 Pulse-width variation with temperature

An important property of delay-line based thermal-sensing is that the usage of 2 closely matched delay-lines causes the systematic process-variations and supply-noise to appear as common-mode noise at the XOR output. A large number of stages for either delay-line plays a significant role towards mitigating the effect of random process-variations on the generated pulse-width. These were the primary reasons for adopting this particular approach towards thermal-sensing since 3-D systems suffer from inter and intra-die process-variations in equal measure and the inherent process-robustness of the design is a much desired attribute.

2.5 Time to Voltage Conversion (TVC)

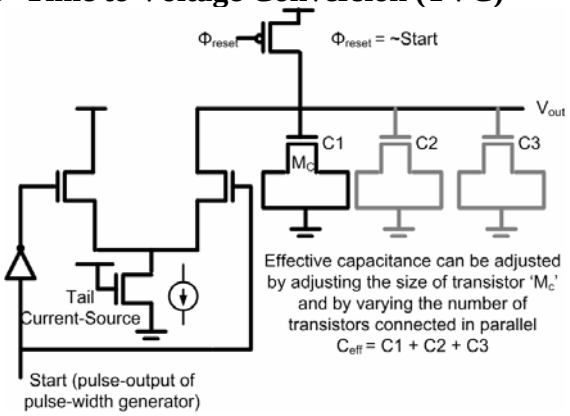

Fig.9: Schematic of Time-to-Voltage conversion circuit [21]

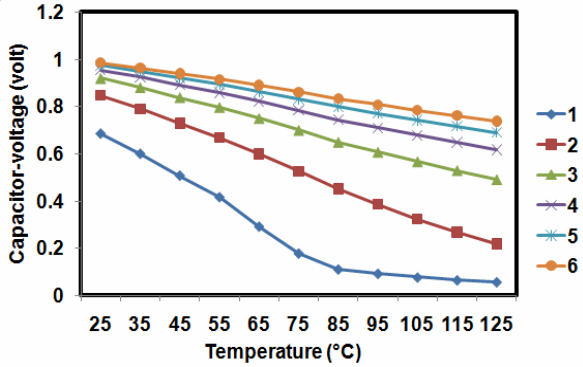

Fig.10: Voltage variation with temperature for different number of capacitors connected in parallel (W_c=20micron)

To convert the variable-width digital-pulse into an analog voltage we used a Time-to-Voltage conversion (TVC) circuit similar to the one proposed in [21]. The output node of the TVC circuit is pre-charged with a pull-up device. The current-steering circuit then discharges the output node as long as the input-pulse is 'high'. Thus, the final-voltage to which the output node settles is directly proportional to the duration of the pulse. The effective capacitance of the output-node can be varied by varying the size of transistor M_C and by having multiple such transistors connected in parallel to increase the effective capacitance of the output node. For a transistor-sizing of 20µ (W_c), we varied the number of cap-transistors connected in parallel and obtained the capacitor-output voltage for the pulse-widths generated at different temperatures (Fig.10). Increasing the effective capacitance of the output node improved the linearity of the response but resulted in a loss of resolution. Thus, we decided on a configuration of two 20µ transistors connected in parallel which provided a resolution of 6.28mV/°C (thermal sensitivity of 1.26%/°C).

2.6 Digitization using Temperature Insensitive Voltage-Controlled Oscillator

For digitization we adopted the VCO-based approach taken in the Itanium Family of processors [15] to save on area/power. Typically current starved VCOs are extremely sensitive to temperature variations and hence can potentially add noise to the sensed temperature-reading during digitization. Therefore, we used a temperature-insensitive design shown in Fig.11 wherein the diode-connected transistors P_1, P_{TS} and N_1 provide temperature compensation to the remaining circuit.

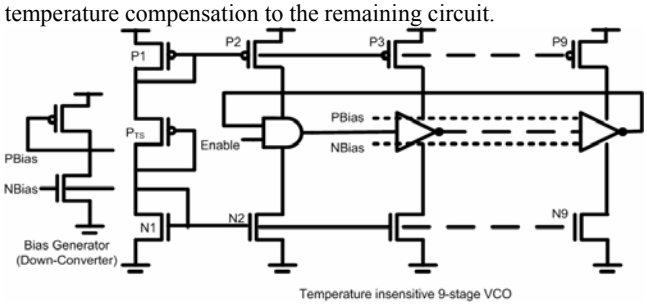

Fig.11: Digitization using temperature-insensitive current-starved 9-stage VCO (V_{OUT} = NBias)

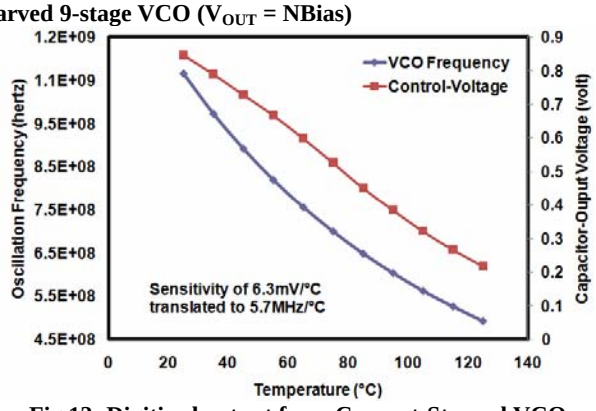

Fig.12: Digitized output from Current-Starved VCO

Transistors P_1 and N_1 were sized in such a manner that the drain current of P_{TS} remained invariant to temperature and hence, the current mirrored into the current-starved branches was also temperature insensitive. This particular VCO design offered a low temperature sensitivity of 0.0071%/ºC as opposed to a sensitivity of 0.79%/ºC observed in a regular current-starved VCO. The sensor output served as the bias for the VCO (N-devices specifically) while bias for the P-devices was generated using a

down-converter. We used a gated VCO wherein the 'start' signal sent out by the controller was used as the 'enable' signal and we performed digitization only when sampling the sensor to minimize power-consumption. The VCO output was found to vary linearly with temperature with a resolution of 5.7MHz/ºC which translated into a thermal sensitivity of 0.82%/ºC (Fig.12). Although the thermal-sensitivity was lesser than that observed for the actual sensing circuit, it was still ~8X of the sensitivity typically observed with on-chip thermal-diodes (~0.1%/ ºC).

2.7 Calibration

For 3-D systems, both inter (D2D) and intra-die (WID) process-variations can cause variation in calibration-constants from one plane to another and inhibit accurate temperature measurement. For our particular design, mismatch in the D2D paths (TSV-wires) will only contribute towards latency-variation of the sensor-response but the thermal-information itself (which is encoded in the signal-frequency) should remain largely unaffected. Thus, from the designer's perspective sensors on all the planes will have *relatively equal* probability to have calibration-error since WID variations are the predominant contributor/source of error for sensor on each plane. In most prediction algorithms, the worst-case reported temperature influences the prediction for the next time-step the most. Thus, to save on tester-cost, a prudent approach will be to calibrate and ensure a more accurate reading for the sensor typically reporting the peak temperatures. For 3-D systems this will be typically the sensor on the plane farthest from the heat-sink. For this plane, calibration will be relatively easier since we can provide a controlled heat-stimulus using a thermal-chuck (i.e. flip the 3-D die and align it with the hot-plate).

3. ANALYSIS OF PROCESS-VARIATION AND SUPPLY-NOISE TOLERANCE

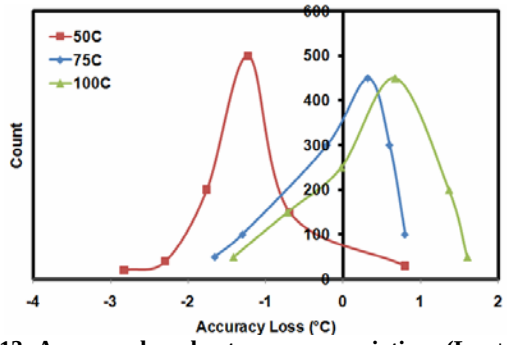

Fig.13: Accuracy loss due to process-variations (L_{eff} + V_{th})

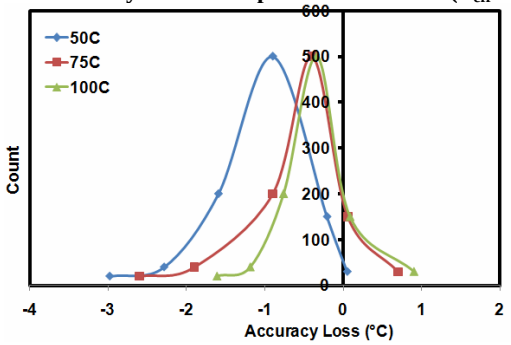

Fig.14: Accuracy loss due to supply-noise

Process variations are the variations in the environmental and physical design parameters which cause the circuit-performance to deviate from its nominal value. For 3-D systems, in order to capture the effect of both inter-die and intra-die variations, we modeled effective channel-length and threshold voltage variations using a Gaussian distribution with a simultaneous 3-σ variation of +/- 15% (instead of the 10% typically used with just intra-die variations and assuming an additive process-impact) and performed 1k Monte-Carlo simulations. HSPICE™ (Synopsys) was the main simulation platform used in our analyses. 65nm technology files were obtained from the PTM website [22]. For each Monte Carlo simulation we determined the deviation from the nominal response caused by the process-variation and then calculated the resultant loss in accuracy assuming 1ºC loss for every 5.7MHz deviation in VCO response. For various temperatures of operation the maximum 1- σ accuracy loss was found to be <= 0.78ºC. To study the effect of random supply noise on sensor performance, we modeled it as a Gaussian distribution with a 3-σ variation of +/-10% and calculated the resultant loss in accuracy at different temperatures of measurement (1ºC=5.7MHz). The 1- σ accuracy loss was found to be <1.06ºC. Thus, our proposed thermal sensing scheme offers a high-level of robustness to both process and supply-noise which is a highly desirable property for thermal-sensors employed in 3-D systems.

4. COMMUNICATION USING TSV

TSVs are the de-facto standard for communication between different strata of the 3-D stack. Since in our sensing scheme, the thermal information is conveyed to the controller plane via the TSVs it is important to quantify the latencies involved in TSV-based communication. We assumed a substrate conductivity and pitch of 10S/m and 25µ respectively and used the RLC parasitic values provided in [23]. In our simulation setup, we used a buffer-horn on each plane capable of driving 50X-INX1 loads (Fig.15). We transmitted a signal of 1GHz (representative of frequency output of VCO from each plane) and measured the latency variation for different temperatures (assuming the same value for all the planes-buffers and the TSVs) and supply-voltages.

Table 1 TSV parasitic values in 65nm [23]

C_g	C_c	L_g	L_m	R_{tsv}
1.89fF	114.2fF	17.13pH	23.27pH	2.78mΩ

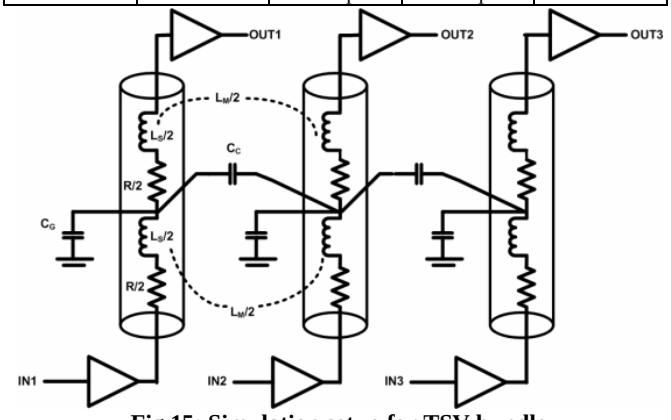

Fig.15: Simulation setup for TSV bundle

Expectedly, the signal latency was found to increase linearly with the increase in number of planes. The slope of the curve became steeper at higher temperatures and lower supply-voltages (Fig.16). The worst-case latency figures must be used to delay the 'enable' signal of the counter used for digitization on the controller plane. In 65nm technology, the worst-case latency for a stack of 10 planes was found to be ~35ps. In our sensing scheme, using dedicated TSVs for each sensor will cause a linear increase in the number of required TSVs with increase in number of planes. This will result in a significant increase in the area/power overhead of

the sensing system since total power-dissipation is dominated by that of the TSV due to the buffering involved (Table 1).

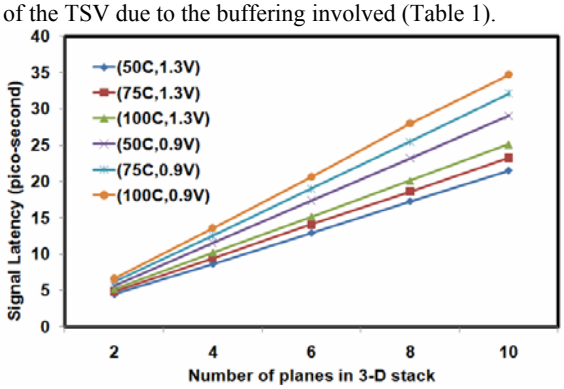

Fig.16: Signal latency variation with number of planes for different temperatures and supply-voltages

Table 1 Power-overhead of design blocks for single sensor

Pul-Gen	TVC	VCO	TSV (2-10 planes)	Total
19.18µW	65 µW	220 µW	360-1340µW	664-1644 µW

Typically, the time-constant of on-chip thermal-events is of the order of ~100ms. This gives us the scope to sequentially sample sensors on individual plane, receive the digitized outputs and store in a register. The sum total of the time-constants involved in the polling of individual sensors and storing their thermal information on the controller plane is an order of magnitude less than 100ms. A very large number of planes can be sequentially accessed for thermal-information within the available time-step (100ms). Sequential access enables us to amortize a small TSV bundle for the exclusive purpose of temperature-monitoring of the entire 3-D system. To access sensors on different planes we need a decoder on the controller-plane but the resultant area/power overhead is nominal compared to the savings achieved by using shared TSVs.

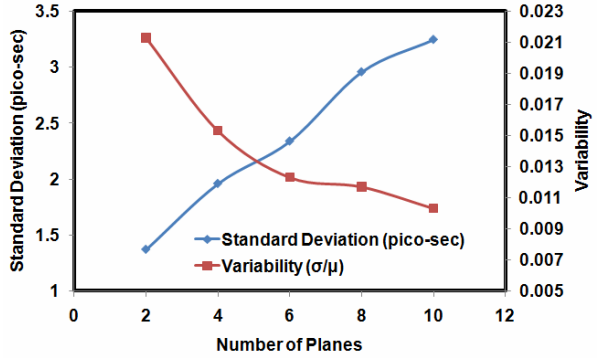

Fig.17: Variability in TSV latency due to process-variations

To assess the impact of random process-variation (in buffer-horn) on voltage-mode TSV-based communication we assumed probability distribution models akin to the ones used in Section 3 and performed 500 Monte-Carlo simulations (with different random variables for each plane) using the simulation-setup shown in Fig.16. While the standard-deviation in latency increased with increase in number of planes in the stack, variability itself decreased. This suggests that stacking more dies in the 3-D stack makes the system more predictable in terms of performance albeit at the cost of higher latencies. Since the σ-values are very small (1- σ <3.5ps) due to usage of large drivers, process-impact on TSV buffers can be largely ignored. The proposed sensing scheme is particularly amenable to TSV-based communication because current/voltage/delay output thermal-sensors are susceptible to attenuation/degradation of logic-levels, while for frequency-output designs, the time-period remains unaffected as long as the noise on the power-delivery network is kept within tight bounds (jitter-free).

5. CONCLUSIONS

In this paper, we have proposed a digital thermal sensing scheme which can be utilized in 3D systems with active temperature control mechanisms. The temperature-sensitive piece is a pulse-generator composed of a pair of delay-lines which provide a large delay-variation per °C change in temperature. It is inherently tolerant towards systematic and random process-variations due to presence of multiple logic-stages, usage of long-channel devices and common-mode noise cancellation. The design is particularly amenable to voltage-mode signaling via TSVs commonly employed in 3-D ICs. The thermal information is transmitted to the controller plane in the form of signal-frequency and hence should remain unperturbed in the absence of jitter in TSV wires. A high post-digitization thermal-sensitivity of 0.82%/°C is achieved and the 1-σ accuracy loss due to process-variations and supply-noise is limited to 0.78°C and 1.06°C respectively indicating a high level of robustness towards process-variations.

6. REFERENCES

[1] A.Coskun et al, "Modeling and dynamic management of 3D multicore systems with liquid cooling", VLSI-SoC, 2009

[2] P.Kapur et al, "Power estimation in global interconnects and its reduction using novel repeater optimization methodology", DAC, 2002

[3] A.Rahman, R.Reif, "System level performance evaluation of three dimensional integrated circuits", IEEE TVLSI, 2000

[4] D.Khalil et al, "Analytical model for the propagation delay of through silicon vias", ISQED, 2008

[5] J.Cong, Y.Zhang, "Thermal via planning for 3-D ICs", ICCAD, 2005

[6] S.Im, K.Banerjee, "Full chip thermal analysis of planar (2D) and vertically integrated (3D) high performance ICs", IEDM,00

[7] A.Coskun et al, "Energy efficient variable flow liquid cooling in 3D stacked architectures", DATE, 2010

[8] A.Rahman et al, "Layout based full chip thermal simulations of stacked 3D integrated circuits", International Mechanical Engineering Congress and R&D Expo, 2003

[9] J.Cong, J.Wei, Y.Zhang, "A thermal driven floorplanning algorithm for 3D ICs", ICCAD, 2004

[10] B.Goplen, S.Sapatnekar, "Efficient thermal placement of standard cells in 3D ICs using a force directed approach", ICCAD, 03

[11] J.Ayala et al, "Through silicon via-based grid for thermal control in 3D chips", Nano-Net, 2009

[12] B.Goplen, S.Sapatnekar, "Thermal via placement in 3D ICs", ISPD,05

[13] J.Cong, Y.Zhang, "Thermal driven multi-level routing for 3-D ICs", ASPDAC, 2005

[14] A.Coskun et al, "Dynamic thermal management in 3D multicore architectures", DATE, 2009

[15] R.McGowen et al, "Power and temperature control on a 90nm Itanium family processor", IEEE JSSC, 2006

[16] V.Szekely et al, "CMOS sensors for on-line thermal monitoring of VLSI circuits", IEEE TVLSI, 1997

[17] P.Ituero et al, "Leakage based on-chip thermal sensor for CMOS technology", ISCAS, 2007

[18] E.Saneyoshi et al, "A 1.1V 35µm x 35µm thermal sensor with supply voltage sensitivity of 2ºC/10%-supply for thermal management in the SX-9 supercomputer", IEEE Symposium on VLSI Circuits, 2008

[19] P. Chen et al, "A time-to-digital converter based CMOS smart temperature sensor", IEEE JSSC, 2005

[20] K.Woo et al, "Dual-DLL-Based CMOS all-digital temperature sensor for microprocessor thermal monitoring", ISSCC, 2009

[21] A.Stevens et al, "A time-to-voltage converter and analog memory for colliding beam detectors", IEEE JSSC, 1989

[22] Predictive Technology Model, http://www.asu.edu/~ptm

[23] R.Weerasekera et al, "On signaling over through-silicon-via (TSV) interconnects in 3-D integrated circuits, DATE, 2010