A Tunable Soft-Error Filtering Circuit Based on Programmable-Threshold Inverters

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***Abstract*—Aggressive device and electrical scaling trends along with the demand for higher operating frequencies have increased the soft-error rate in sub-100nm combinational logic. Mitigation techniques proposed at the circuit-level include glitch-filters which suppress the propagated transient before it gets latched to a memory-element but these typically have a significant performance overhead (>=50ps) during normal operation. In this paper, we propose a tunable filtering circuit based on programmable-threshold inverters. The logic-threshold of the filter can be adjusted statically, by device-sizing, as well as dynamically, by setting appropriate configuration-bits. In 45nm technology, it has a low delay and power overhead of <12ps and < 9µW respectively and occupies a small area of 23.56µ^2. The design is robust towards process, voltage and temperature variability retaining full functionality for a 3-σ variation of +/-10% in process-parameters and supply-voltage and over a temperature range of 25-125ºC.**

I. INTRODUCTION

A combination of technology scaling trends, which includes decrease in node-capacitance and supply-voltage with every generation, and micro-architectural practices in high performance nodes, which includes increase in clock-frequencies and super-pipelining of paths reducing logic-depth, has drastically increased the susceptibility of nanometer designs to transient faults caused by soft-errors [1][2][3]. A soft-error is a transient error in the result of a combinational circuit which may get subsequently latched to a memory circuit resulting in a transient fault. Soft-errors occur due to single-event transients (SET) caused by neutron strikes from atmosphere and high-energy alpha particles from IC packaging material [3]. These particle strikes generate a current-pulse at a circuit-node which 'may' produce a voltage-glitch at the gate-output depending on: energy of incoming particle, geometry of impact, location of strike and logic design style employed [1][2]. Typically, a soft error manifests itself as a bit-flip in a memory element [4][5] but recent projections [6] indicate that the soft-error rate (SER) of combinational logic is expected to rise by 9 orders of magnitude from 1992 to 2011 and become comparable to the SER of unprotected memory elements. Combinational circuits have inherent masking mechanisms which suppress glitch-generation and propagation. The efficacy of these masking mechanisms: logical, temporal and electrical, is significantly reduced in deep nanometer nodes [2] and hence explicit design solutions are needed. The standard error detection and correction techniques used to enhance the reliability of memory include hardware-redundancy [7], timing redundancy [8] and logic rewiring [9]. These however have limited usage in combinational circuits because the irregular topology will make the design overhead prohibitively high. Hence, gate-level and circuit-level radiation hardening solutions are needed for combinational logic.

At the gate-level, the techniques proposed in literature typically tune design parameters like sizing and supply-voltage to improve gate-robustness to SETs. In [10], critical gates are selectively sized while in [11], a capacitive load is added to the primary outputs followed by gate-size modification and VDD assignment of internal gates to achieve SET robustness. In [12], an optimization framework based on geometric programming has been proposed to perform optimal assignment of size and VDD. A technique based on simultaneous gate sizing and flip-flop selection has been proposed in [13]. At the circuit-level, several filtering circuits have been proposed to mask SET transients. A glitch filter utilizing the low pass filtering characteristics of pass-gates has been proposed in [14]. In [15], vulnerable gates are duplicated and the outputs of the original and shadow gates are connected using a voltage-clamping circuit to prevent SETs from affecting the output voltage. In [1], a soft-error masking circuit based on a Schmitt Trigger circuit has been proposed. Pass transistors are used to reduce the magnitude of the transient pulses followed by a Schmitt Trigger to completely mask the glitch. All these filter designs however incur a very high performance penalty since the filtering circuits are added post-synthesis. A tunable transient filter (TTF) has been proposed in [3] which can be tuned during design based on the criticality of the path in which it is placed and the magnitude of SET that needs to be suppressed. Even in its minimum possible configuration, the TTF incurs a very high performance penalty of 50ps.

In this paper, we propose a tunable glitch filter based on programmable threshold inverters (PTI). The proposed design

suppresses propagated glitches before they can be captured by memory elements and can be tuned to adjust the maximum amplitude of the input SET that needs be suppressed. A single unit of this design is constructed using 12 transistors only and has a very low performance overhead of <12ps. The rest of the paper is organizes as follows. In section 2, we describe the functionality of our tunable filter, our simulation setup and the basic characteristics in terms of glitch suppression. We discuss how tunability is achieved through different configurations and sizing. In section 3 we analyze the robustness of out filter to PVT variability and finally in section 4, we present our conclusions.

II. GLITCH FILTERING USING TUNABLE FILTERS

A. Soft Error Models for Logic Circuits

The high energy neutron and alpha particle strikes responsible for causing soft-errors have a uniform spatial and temporal distribution [4]. With the advent of improved packaging technologies, soft-errors caused by alpha particles have drastically reduced. For neutron strikes several device level models have been proposed in literature to model the charge deposition at random circuit nodes. The most popular circuit-level model is the double-exponential model proposed in [17]. It's a simple model which requires the charge deposited (Q) and the rise-time (ζ_r) and fall-time (ζ_f) constants for the current glitch produced by the particle strike.

$$I_{in}(t) = \frac{Q}{(\zeta_f - \zeta_r)}\left(e^{\frac{-t}{\zeta_f}} - e^{\frac{-t}{\zeta_r}}\right) \quad (1)$$

Since we were mostly concerned with the masking of a propagated glitch, we modeled a propagating SET with a trapezoidal pulse with rise and fall times of 15ps at the inputs to the filter. We considered a SET to be sufficiently attenuated if the filtered pulse amplitude was less than 0.2V (for positive glitches) or more than 0.8V (for negative glitches). The simulation setup consisted of 45nm models obtained from PTM and all simulations were performed using HSPICE.

B. Tunable Glitch-Filter Design

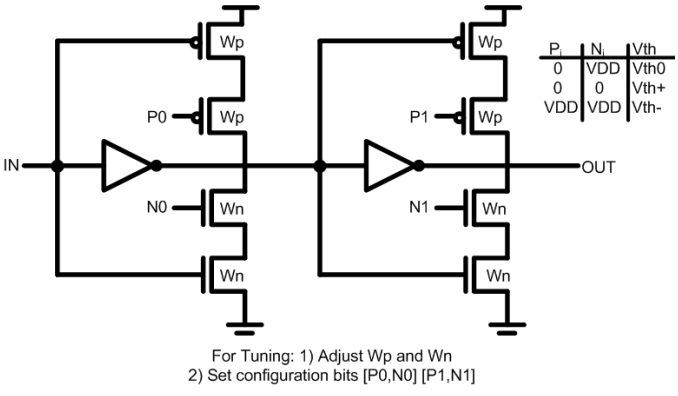

Figure 1. Schematic of programmable-threshold inverter (PTI) based filter

Filter-designs based on pass-gates suppress input pulses that are of smaller width than their own inertial delay [3]. The problem with this approach is that the hardware overhead of this design depends upon the size of the glitch being suppressed as the number of pass-gates required will increase linearly with the glitch-width. A Schmitt Trigger based approach utilizes its hysteresis property thereby suppressing glitches that fail to cross the logic thresholds [1]. Such a design however cannot be tuned since the device-sizing fixes the logic-threshold values. To overcome these issues in glitch-filter design we propose a filter using a combination of two programmable threshold inverters (PTI) (Fig.1). The logic-threshold values of the programmable threshold inverter can be tuned by: 1) Adjusting the sizing of the PMOS and NMOS devices (W_p/W_n) 2) Setting appropriate configuration bits (P_i, N_i). The filter consists of 2 such inverters that work in conjunction to suppress a glitch. Depending upon the configurations bits, each inverter has the following two threshold voltages: a rising input threshold voltage (Vth+) and a falling input threshold voltage (Vth-). The output of the inverter switches from low to high only when the input voltage is higher than Vth+ and switches from high to low only when the input voltage is lower than Vth-. As a result, glitches of amplitude lower than Vth+ do not affect the output at logic-0 state and those of amplitude higher than Vth- do not degrade the logic-1 state of the output. By using 2 PTIs we ensure that the filter is non-inverting and also, its efficacy towards glitch-filtering is improved as we use complimentary configurations bits for the 2 inverters making the effective threshold value even higher/lower for positive/negative glitches. The figures below illustrate the attenuation characteristics of our design. We have assumed a glitch-width of 60ps and set configuration bits as [P=0, N0=0, P1=0, N1=1] and [P=1, N0=1, P1=0, N1=1] for the positive and negative glitches respectively.

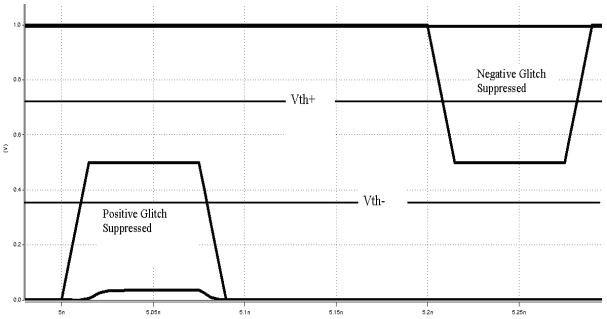

Figure 2. Suppression of tranisent pulses by masking circuit

The effective threshold of the filter can be adjusted by setting the configuration bits according to the transient error susceptibility of the path under consideration. The delay/power overhead of the filter is affected by the configuration bits being used. While a high rising input threshold (Vth+) followed by a low falling input threshold (Vth-) yields the best result for positive-glitches, an opposite configuration of Vth- followed by Vth+ yields the best results for a negative glitch. The best possible configurations to suppress positive and negative glitches (in terms of the resultant amplitude of the filtered signal) have been shown in Fig.3. Unlike traditional pass-gate based filters, the width of the transient has no effect on the filtering characteristics of the design. The charge deposited directly impacts the peak-amplitude of the current-pulse while the time-constants associated with charge-decay are primarily set by the device characteristics. Since in scaled nodes the critical charge required to exceed the natural logic threshold of the gate is very small it is important to have fine-grain control over the logic-threshold values of the filter and the glitch-duration

which is directly affected by process and environmental parameters should have no effect on filtering characteristics.

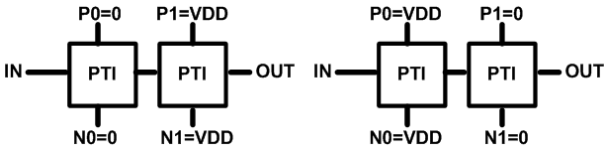

Figure 3. Filter configuration for suppression of (i) positive and (ii) negative glitch

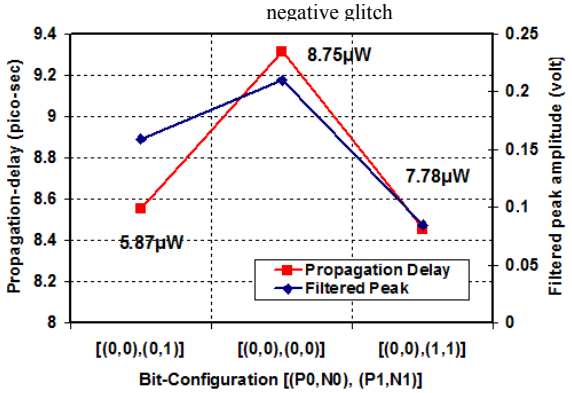

Figure 4. Filtering characteristics for positive glitch-suppression with delay/power overhead (input glitch peak = 0.56V)

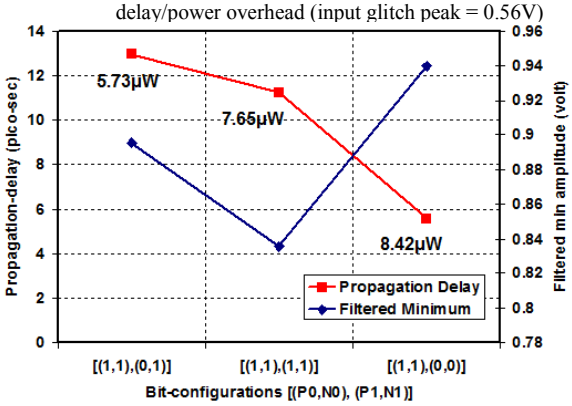

Figure 5. Filtering characteristics for negative glitch-suppression with delay/power overhead (input glitch minimum = 0.44V)

Figures 4 and 5 indicate the area/overhead for the bit-configurations which yield the best results for positive and negative glitch suppression. The logic-threshold of the filter can also be tuned by changing the device-widths. By setting the filter-threshold to 0.2V (for positive-glitch), we progressively increased the device-widths of the filter and determine the maximum input glitch amplitude that could be suppressed and computed the corresponding power-overhead. Expectedly, the logic threshold increased with increase in device-width (for the bit-configuration selected) and so did the peak-amplitude of the filtered input-glitch (~7.6% per 1X increase). The corresponding power-consumption increases super-linearly (~38% per 1X increase) and hence upsized devices must be used only when the transient-error vulnerability of a path is very high and a strict control over the allowable noise-margin is required. If we consider the minimum sized configuration then for a low power and delay-overhead of < 9µW and <12ps respectively, both positive and negative glitches can be suppressed which is far lesser than the numbers reported by contemporary designs. In addition, there is also scope to tune the design to adjust the filter-threshold which is useful for multi-core designs having variable architectural vulnerability factors. The proposed filter has a relatively compact layout occupying 23.56µ^2 in 45nm technology using CMOS-SOI models (Fig.7).

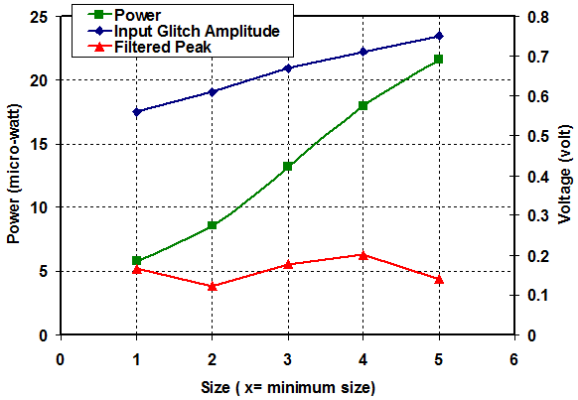

Figure 6. Filtering characteristics for upsized filters and corresponding power overhead (positive-glitch suppression)

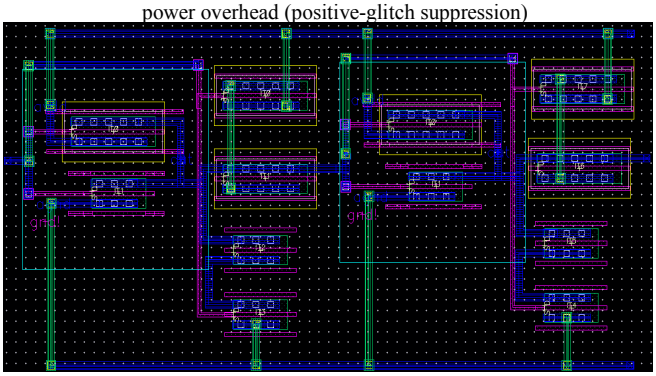

Figure 7. Layout of tunable glitch-filter using 45nm CMOS-SOI models

III. IMPACT OF PVT VARIABILITY ON FILTERING CHARACTERISTICS

Process variations are the variations in the environmental and physical design parameters which cause the circuit-performance to deviate from its nominal value. Environmental variables are the dynamic operating parameters such as temperature and supply-voltage. Intra-die physical variations include variations in device electrical parameters - effective channel-length (L_{eff}), threshold-voltage (V_{th}), gate-oxide thickness (T_{ox}) and drain/source parasitic resistance (R_{dsw}) and variation in interconnect-dimensions.

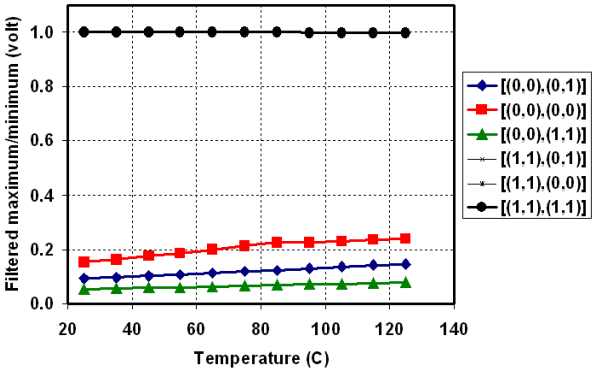

Fig.8 Thermal impact on max/min amplitude of filtered glitch (positive/negative glitch suppression)

To study the effect of temperature rise on the filtering characteristics, we varied the temperature from 25ºC to 125ºC

(operating range of processors) and measured the filtered maximum or minimum for different configuration-bits settings. There was no effect of temperature on the negative-glitch filtering characteristics. In the case of positive-glitches, the filtered peak gradually increased with temperature for all configurations but still remained lower than the acceptable threshold for logic-0 (0.2V). The increase in filtered-peak was due to relative dominance of threshold-voltage effect in our filter design which caused an increase in device drain current with temperature (Fig.8).

To study the effects of intra-die process-variation on the response of proposed filter, we modeled effective channel-length and threshold voltage variations using a Gaussian distribution with a maximum variation (3-σ) of +/- 10% and performed 1k Monte-Carlo simulations. HSPICE™ (Synopsys) was the main simulation platform used in our analyses. 45nm technology files were obtained from the Predictive Technology Model website [16]. For all the different configurations used for positive glitch suppression the entire distribution of the filtered peak remained less than 0.2V thus indicating successful filtering even in the presence of process-induced variability. The mean of the distribution shifted according to the configuration bits being applied with μ_{min} obtained for [P0 = 0, N0 = 0, P1 = 1, N1 = 1]. (Fig.9)

Table 1 Device Parameters and +/-3σ variations in 45nm

Parameter	Nominal + 3σ deviation
L_{eff} (nm)	17.5 +/- 10%
V_{th} (V)	(0.466,-0.418) +/- 10%

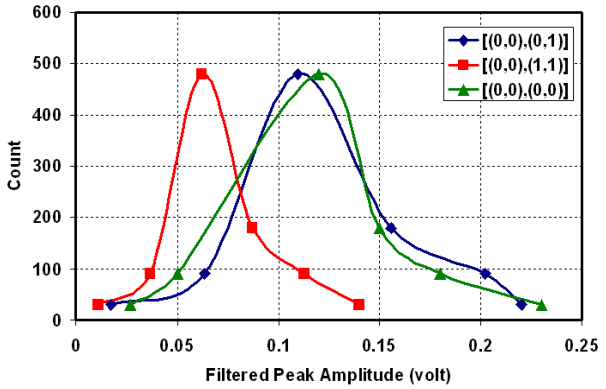

Fig.9 Distribution of filtered peak amplitude for different configurations used for positive glitch suppression under process-variation

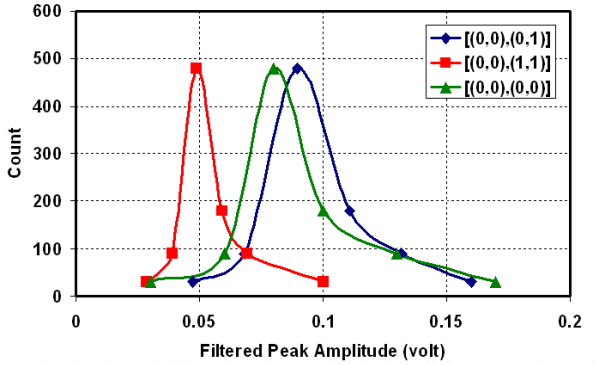

Fig.10 Distribution of filtered peak amplitude for different configurations used for positive glitch suppression in the presence of supply-noise

As CMOS feature sizes shrink and device integration density increases, on-chip power supply droop caused by large dI/dt becomes an increasing concern. To study the effect of random supply noise on sensor performance, we modeled it as a Gaussian distribution with a 3-σ variation of +/-10%. The entire filtered-peak distribtion was <0.2V for all possible configurations used in positive glitch suppression indicating a high level of tolerance to supply-noise as well (Fig.10).

IV. CONCLUSIONS

In this paper, we have presented a glitch-filtering circuit, capable of masking transients of the order of 0.56V (positive-glitch) and 0.44V (negative glitch). The logic threshold of the filter can be tuned by both device sizing as well as by setting appropriate configuration bits depending upon the soft-error vulnerability of the path under concern. The proposed design has a low delay and power overhead of <12ps and < 9μW respectively and has a relatively low area of 23.56μ^2 in 45nm CMOS-SOI technology. The design is also relatively robust towards variations in process-parameters, supply-noise and temperature as its functionality remains intact in the presence of a 3- σ deviation of +/-10% in the process/supply parameters and over a temperature range of 25-125ºC.

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