

Robust Signaling Techniques for Through Silicon Via Bundles

Krishna C Chillara
ECE Department
University of Massachusetts
Amherst MA USA 01002

kchillara@ecs.umass.edu

Jinwook Jang
ECE Department
University of Massachusetts
Amherst MA USA 01002

jjang@ecs.umass.edu

Wayne P Burleson
ECE Department
University of Massachusetts
Amherst MA USA 01002

burleson@ecs.umass.edu

ABSTRACT

In high performance 3D ICs with increasing trend for multi-core and NoC architectures, signaling techniques play a crucial role in determining the overall performance of the system. In this work, we explored single ended and differential signaling techniques for Through Silicon Via (TSV) bundles and analyzed their behavior in the presence of power supply noise. We obtained maximum data rate and energy/bit values for each of the signaling techniques and identified the dominant factors that determine these values. Simple analysis is carried out to understand the impact of fault tolerant scheme on the performance of the signaling technique. Frequency dependent RLGC parasitics of 3x3 and 4x4 TSV bundles are extracted using Ansoft Q3D Extractor. NCSU 45nm PDK and HSPICE simulation tool are used. For robustness to supply noise analysis, noise amplitudes of 2.5%, 5%, 7.5% and 10% of supply voltage and a noise frequency of 200MHz is considered. It is observed that Inter Symbol Interference (ISI), power supply noise and fault tolerant architecture play crucial role in determining the robust and high performance signaling technique for TSV bundles.

Categories and Subject Descriptors

B.7.1 [INTEGRATED CIRCUITS]: Types and Design styles – *Advanced technologies.*

General Terms

Design, Performance.

Keywords

3D Integrated Circuits, Through Silicon Via, Voltage Mode, Current Mode, Single Ended and Differential techniques.

1. INTRODUCTION

In recent years, 3D IC design is gaining significant attention as a possible solution to the problem of Interconnect Bottleneck. TSV based 3D ICs are crucial in designing high density systems and therefore it is important to understand the electrical properties of

TSVs. Some of the earlier work on TSV characterization has been carried out by Savidis et al. in [1], using Ansoft Q3D extractor. In [2], Pak et al. studied the impact of structural and material parameter variations on RLC values for parallel TSVs. TSV bundles are found to provide better yield [3] and the first work on TSV bundles focusing on crosstalk is presented in [4]. In [5], Weerasekera et al. explored single ended voltage mode and current mode signaling techniques for 3 parallel TSVs. In [6], LVDS based differential signaling and LVSE based single ended signaling schemes are explored for parallel TSVs.

In this work, we focused on digital CMOS applications where the substrate conductivities are significantly high [5] and observed that the impact of crosstalk is negligible compared to the Inter Symbol Interference. We then present a simple analysis to understand the impact of fault tolerant scheme on signaling. Considering the significance of power supply noise in 3D ICs, robustness of the signaling techniques to supply noise is analyzed.

The paper is organized in the following manner. Section 2 deals with TSV modeling with two subsections, one on RLC parasitic extraction and their frequency dependency and the second subsection on fault tolerant schemes and the tradeoffs involved. Section 3 will discuss the single ended voltage and current mode signaling techniques. Differential current mode signaling technique is explored in Section 4. Robustness analysis in terms of impact of power supply noise and fault model is presented in Section 5. Section 6 concludes the paper.

2. TSV MODELING

2.1 RLC parasitics of TSV

The RLGC parasitics of copper filled TSV bundles for upto 35GHz are extracted using Q3D extractor [7]. The schematic of the structure of TSV bundle is shown in Fig.1 and its RLGC values at DC and 2GHz frequency are mentioned in Table 1. The TSVs used in this work, have the diameter of 10 μ m, length 25 μ m and pitch (twice the diameter) 20 μ m. TSVs are coated with a thin dielectric (SiO₂) layer of 0.2 μ m thickness. Dielectric layer is used to prevent any DC leakage of currents into the substrate. In Table 1, Ls and Cs represent the self inductance and capacitance values respectively. The values under Lm and Cc represent the mutual inductance and coupling capacitance with one of the immediate non diagonal neighbors. It can be seen that self capacitance dominates over coupling capacitance due to the dielectric coating around the TSVs and high substrate conductivity acting as a shield. The mutual inductance values decrease gradually from immediate neighbor to the next neighbor. Fig. 2 shows the variation of R, G and L with frequency.

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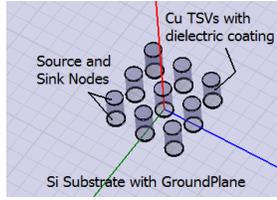


Figure 1 Q3D Extractor Schematic of 3x3 TSV Bundle.

Table 1 RLC values from Q3D Extractor

Freq	R (mΩ)	Ls (pH)	Lm (pH)	Cs (fF)	Cc (fF)
DC	4.88	7.14	2.25	116.34	0.01
2 GHz	16.38	5.66	1.38	116.34	0.01

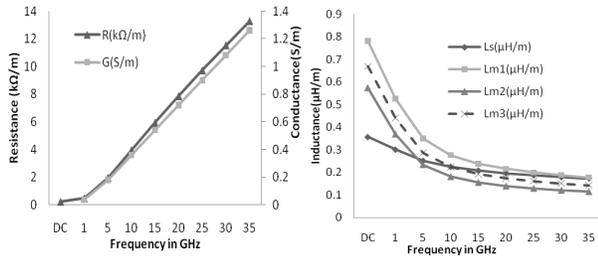


Figure 2 Linear variation of R, G and Inverse variation of Inductance with frequency

The resistance increases and the inductance decreases with the frequency due to skin effect. The effective conductivity of material increases with frequency, hence increasing the conductance as observed in Fig. 2. In a 3x3 TSV bundle, the mutual inductance experienced by a TSV depends on its location. Lm1 represents the mutual inductance at Center TSV; Lm2 for 4 corner TSVs and Lm3 represents the mutual inductance of rest of the TSVs. The center TSV has 8 immediate neighbors, thus experiencing the maximum coupling compared to other TSVs.

2.2 TSV Fault tolerance

Although Through Silicon Vias are excellent electrical conductors, a failed TSV can cause a number of known good dies that are stacked together to be discarded. Redundancy based fault tolerant schemes provide a simple and efficient solution [3]. In this section a simple analysis is carried out on redundancy based fault tolerant architectures with particular focus on their impact on high speed signaling techniques. Fig. 3 shows three possible approaches of redundancy based fault tolerant architectures obtained by changing the relative positions of serializer (Ser), fault recovery multiplexer (MUX) and the driver circuits. The redundant TSV (R_TSV) and faulty TSV are shown in Fig.3. Fault tolerant model A, as shown in Fig. 3 (a) is a simple solution consisting of a Serializer, followed by a driver followed by one bit 2x1 MUX or the delay cells. The major issue with this approach is the dependency of the MUX and delay logic implementation on the signaling scheme. For example, differential signaling with Current Mode Logic (CML) driver needs the MUX and delay cells to be implemented in CML compatible logic. In order to utilize these excellent but scarce TSVs efficiently it is important to operate at the maximum data rate through TSV that can be supported by a particular signaling technique. Thus, this approach necessitates the design of fault recovery MUX and delay cells to support such high speeds resulting in an increased design complexity and power consumption.

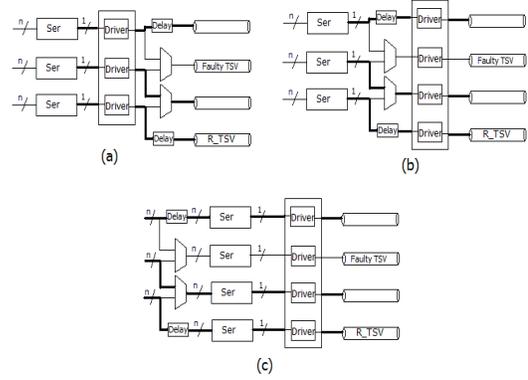


Figure 3 Redundancy based fault tolerant architectures

(a) Final stage MUX based approach (b) Driver decoupling MUX and TSV approach (c) MUX before Serializer approach

In approach B, as shown in Fig. 3(b), it can be observed that the MUX and the delay cell logic can be implemented independent of the signaling technique and the implementation logic of the driver. This comes with an overhead of additional driver circuit for redundant TSV. This approach still necessitates the design of fault recovery MUX and delay cells to be able to operate at higher data rates supported by the TSVs. In approach C, as shown in Fig. 3(c), the multiplexing is moved before the serialization block. This facilitates the design of MUX and delay cells that can operate at the data rates that are 'n' times smaller than the signal data rates through the TSVs, thus reducing the power and design complexity. The overhead involves an additional Serializer and the driver circuit for the redundant TSV. Also one bit 2x1 MUX and delay cells are now replaced with 'n' bit 2x1 MUX and 'n' bit delay cells. Thus depending on the signaling technique, an optimum fault tolerance scheme should be determined considering the above tradeoffs. In the next section we explore the maximum data rates that can be supported by single ended and differential techniques. In Section 5, we assume Fig. 3 (c) as the fault tolerant architecture, and show the impact of TSV faults on the signal quality.

3. SINGLE ENDED TECHNIQUES

3.1 Voltage Mode Signaling

In this subsection, the maximum data rate using Single Ended Voltage Mode (SEVM) signaling technique for TSV bundles is obtained. Each TSV of the 3x3 bundle is driven by the 64 x inverter driver. At the receiver end, a unit inverter with FO4 load is considered. The simulation setup for one of the TSVs in 3x3 bundle is shown in Fig. 4.

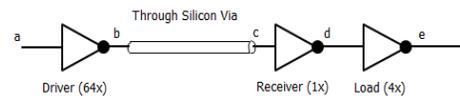


Figure 4 Voltage Mode Simulation Setup for one of the TSVs

The center TSV will experience the maximum coupling in the bundle and hence all the simulation results are taken at the nodes of this TSV. Simulations are performed in HSPICE using $2^7 - 1$ Pseudo Random Bit Sequence (PRBS) with 10ps rise and fall time as inputs. The eye diagrams are plotted at the output of the 1x receiver, node 'd'. Targeting an eye height of 60% of VDD as

considered in [2], the maximum data rate that can be supported by voltage mode signaling is found to be 24.4 GBPS. It has an eye height of 0.67V and eye width of 33.8ps. The energy per bit for voltage mode signaling considering both driver and receiver circuits is found to be 1.867fJ/bit.

3.2 Current Mode Signaling

In this section, the current mode or low impedance mode signaling schemes are designed and analyzed. Similar to voltage mode, a 64x inverter is used as driver. The simulation setup for current mode analysis is shown in Fig. 5. The receiver circuit here has a low impedance node compared to a high input impedance of inverter which is used in voltage mode. In this work, we first analyze the circuit presented in [5] with loading on the receiver side which is not considered in [5]. Let us call this circuit as Current Mode Receiver 1 (CMR1) and the signaling as Single Ended Current Mode 1 (SECM1) signaling. Then we modify the receiver circuit as described in [8]. Modified receiver circuit is called Current Mode Receiver 2 (CMR2) and the signaling as Single Ended Current Mode 2 (SECM2) signaling.

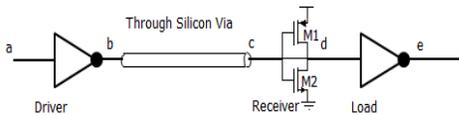


Figure 5 Simulation Setup for SECM1 Signaling

In Current mode signaling, the improvement in performance is mainly due to the reduced signal swing at the receiver. Considering the CMR1, the sizing of M1 and M2 plays a crucial role in determining the signal swing at the output. As the size of M1 and M2 transistors increases, the signal swings decrease thus increasing the speed. But this improvement in speed gradually decreases and the link fails once the signal levels are too low to switch the load inverter. From simulation results for maximum speed, the size of M1 and M2 are chosen to be 64x unit size in 45nm CMOS technology. Similar to voltage mode simulations, the inputs to the 3x3 TSV bundle are provided by the $2^7 - 1$ PRBS with rise and fall times of 10ps. Considering 60% eye height, the maximum data rate is found to be 42.2 GBPS. The energy per bit for current mode signaling with CMR1 is found to be 0.527fJ/bit.

Performance improvement to the receiver circuit of CMR1 can be obtained by adding an NMOS transistor between the nodes 'c' and 'd'. This circuit is introduced in [8] where the signaling mode switches from current mode to voltage mode depending on the transition in the incoming data signal. In this work, we bias it to a fixed voltage such that the transistors M1 and M2 are in saturation region and operate at the maximum feedback gain. This increased gain also helps in reduction in the overall impedance due to Miller effect. As the size of bias transistor increases the gain increases but at the same time, the drain and source capacitance also increases. Hence the improvement in performance with increase in the transistor size gradually decreases due to the increasing capacitance. Based on the simulation results the transistor size is chosen to be 64x unit NMOS in 45nm CMOS technology node. The maximum data rate for CMR2 is found to be 49.7 GBPS. The energy per bit for this scheme is 0.301fJ/bit. In comparison to CMR1, 57% improvement in energy/bit is achieved.

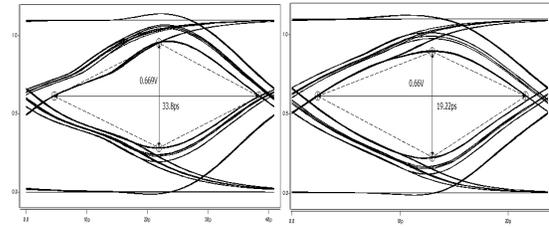


Figure 6 Eye diagrams of single ended techniques-SEVM at 24.4 GBPS and SECM1 at 42.2 GBPS

4. DIFFERENTIAL TECHNIQUE

In 3D ICs, the variation in currents drawn in one tier can impact the supply nodes in adjacent tiers resulting in an increased dynamic noise [9]. Single ended signaling schemes which consider VDD and VSS as high and low voltages suffer significantly due to power supply noise, thus motivating to explore differential technique. In view of the advantages of current mode over voltage mode in terms of high performance and its ability to detect very low output swings, Differential Current Mode (DCM) signaling as shown in Fig. 7 is considered in this work. The differential inputs are applied to the gates of the transistors M1 and M2, which are pinned to carry a total current of 1mA with the help of a tail current source. At the receiver side, a simple common gate transistor with a load resistor is used for each leg. Thus, depending on the differential inputs, the current in one of the legs dominates over the other resulting in differential outputs. The bias voltage is applied so that the transistors operate in saturation region. Such a receiver configuration with a simple common source driver is explained in [10]. Simulations are performed using $2^7 - 1$ PRBS inputs.

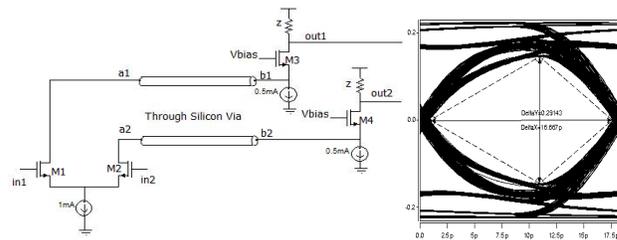


Figure 7 Circuit schematic of Differential Signaling circuit and its eye-diagram with one-bit pre-emphasis at 55GBPS

Significant ISI was observed at the output node resulting in a reduced eye opening of 105mV eye height and 9.82ps eye width. Following this observation, a simple one bit emphasis is used to improve the signal quality. Improved eye diagram with an eye height of 291.43mV and eye width of 16.667ps is shown in Fig. 7. The energy per bit for differential signaling is 0.389fJ/bit.

5. ROBUSTNESS ANALYSIS - IMPACT OF SUPPLY NOISE AND TSV FAULTS

For robustness analysis, impact of supply noise and TSV faults is analyzed. In this work, global power supply noise of 200MHz frequency as mentioned in [11] is considered. Since the power supply noise amplitudes in 3D ICs can be as high as 10% of the supply voltage [9], simulations are performed considering the noise amplitudes of 2.5%, 5%, 7.5% and 10% of VDD. For each

signaling scheme, normalized values of eye height and eye width are obtained by comparing them with those obtained with ideal supply voltage conditions. Impact of supply noise on each of the signaling schemes as indicated by the variation in the eye width and eye height is shown in Fig. 8. It can be observed that single ended signaling schemes experience upto 20% reduction in eye width and upto 35% reduction in eye height. This indicates that single ended techniques are highly affected by the supply noise variations when compared to differential technique. Among single ended techniques Voltage mode is more affected compared to Current mode as indicated by the significant reduction in eye parameters for SEVM.

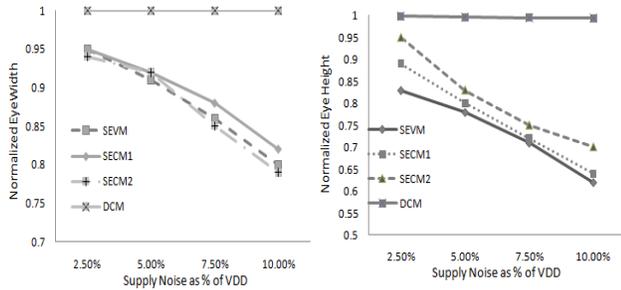


Figure 8 Supply Noise reducing the eye opening in single ended techniques while no impact is observed in differential.

Assuming the fault tolerance scheme as described in Fig. 3 (c), simulations are performed to understand the impact of faulty TSV in a 3x3 bundle. The faulty TSV can be stuck at 1, stuck at 0, short circuited to other net or open circuited. The eye height and eye width on the center TSV under ideal case and those when one of the TSVs is stuck at VDD, VSS or open circuited for SEVM are obtained. We observed a very little variation of 0.05% in eye width and 0.06% in eye height, indicating a very little impact of the faulty TSV on the normal TSV. This is primarily due to the low coupling capacitance values between the TSVs.

6. CONCLUSION

In this work, we explored various signaling schemes for 3D TSV bundles. In 3D ICs with high substrate conductivities, we observed that Inter Symbol Interference and power supply noise are more dominant problems than crosstalk due to coupling. With simple analysis we explained the tradeoffs involved in the design of redundancy based fault tolerant schemes. The eye height and eye width values under ideal supply voltage conditions and with supply noise amplitude of 10% VDD are presented in Table 2. It can be observed that the bandwidth per TSV of differential signaling is 50% of its maximum data rate (55GBPS) as it requires two TSVs per signal. Though differential signaling scheme has slightly higher energy/bit value (0.389fJ) compared to SECM2 (0.301fJ), considering its robustness to supply noise, differential technique is found to be more optimum signaling technique for TSV bundles.

Table 2 Impact of supply noise on signaling schemes

Signal Scheme	Energy /Bit (fJ)	BW/ TSV (GB PS)	Eye Height (V)		Eye Width (ps)	
			Full swing	10% noise	Full swing	10% noise
SEVM	1.867	24.4	0.66	0.42	33.8	27.1
SECM1	0.527	42.2	0.66	0.43	19.2	15.8
SECM2	0.301	49.7	0.66	0.46	13.8	10.9
DCM	0.389	27.5	0.29	0.29	16.7	16.7

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