A 45.6μ² 13.4μW 7.1V/V Resolution Sub-Threshold Based Digital Process-Sensing Circuit in 45nm CMOS

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ABSTRACT
Process optimization and yield enhancement techniques rely on physical sensors to provide them with feedback to perform accurate process-characterization across the die. The increased susceptibility of circuit performance characteristics to parameter variations in deep sub-micron technologies motivates the need for low-overhead (area/power) and high-sensitivity process monitoring circuits which can be used by compensation schemes to tune the process and meet frequency targets or power-budgets. To this end, we have proposed and implemented in 45nm CMOS-SOI, a novel, digital, on-chip process sensing circuit with a high sensitivity of 7.1V per volt variation in NMOS V_{th}, low power dissipation of 13.4μW and a compact layout occupying 45.6μ². The design is robust towards temperature variations and supply induced noise incurring an accuracy loss of 5mV (worst-case) and 4mV (1-σ) respectively of the NMOS threshold-voltage.

Categories and Subject Descriptors
B.7 [Integrated Circuits]: Types and Design Styles

General Terms
Measurements, Design

Keywords
Process-variation, sensor, sub-threshold operation

1. INTRODUCTION
The ever increasing need for higher operating frequencies and increasingly complex chip functionality have been the driving force behind aggressive scaling of transistor dimensions. The increase in integration density has enabled system-designers to reap the power/performance benefits of scaling but the want of greater functional complexity in current generation ICs has ensured that the die-sizes continue to grow larger. A few recent examples of this paradoxical phenomenon include the Intel Pentium III Tualatin which packs a few million transistors in 80mm² area in 0.13-μm process and the Intel Core 2 Quad Kentsfield processor which has half a billion transistors in 286 mm² in the 65nm process [1]. Larger dies with yet larger number of transistors significantly aggravate the role of process-variation in undermining circuit robustness. The primary circuit-parameter affected by random process-variations is the threshold-voltage of the devices. Variation in circuit performance induced by variability in device threshold-voltage can potentially lead to parametric/functional failures degrading the manufacturing yield. Intra-die threshold variations have been shown to adversely influence path-delays of low-voltage digital circuits [2] and consequently, cause glitches and clock-skew. Thus, it is imperative to effectively sense/track the random variation in threshold-voltage and provide feedback to process-compensation techniques which can then tune the process and enhance manufacturing yield [3] [4][5].

Static parameter variations are of 2 types: inter-die and intra-die [6]. While the former affects all transistors of a die uniformly the latter can be further sub-divided into 2 components – systematic and random. Systematic intra-die variations tend to have strong spatial correlation for devices in close vicinity as shown by the Pelgrom Model [7] and adaptive body bias (ABB) is a technique frequently employed to compensate for such variations [8]. Random process variations which are caused by Line Edge Roughness (LER) and Random Dopant Fluctuation (RDF) [6] offer no spatial correlation and become significant in the scaled technologies. Random variations can cause fluctuations in circuit parameters to degrade both performance and yield. The effect of random variations is particularly severe on SRAM bitcells which are composed of minimum sized transistors and hence susceptible to failure caused by degradation of read/write stability. Accurate estimation of process-corner in a closely-spaced region is crucial to perform process-optimization and ensure valid operation of circuits in that region. It has been shown that adaptive biasing of digital circuits based on threshold voltage estimation can improve their yield from 14% to 86% in 130nm process technology [9].

The traditional approach to process characterization was to determine the IV-curves of multiple neighboring devices under test (DUT) by multiplexing them to pads [10]. This technique is limited by the number of available pads and also, requires extensive data-analysis to follow accurate current measurement [3]. Ring oscillators have been proposed in [11] to measure variability statistics but such a technique will be constrained by the large area/power overhead of the ring-oscillator circuit. In [12], a leakage-sensing circuit has been proposed to provide process compensation to dynamic circuits but it requires variation independent biasing circuits that cause unnecessary area overhead. A sense-amplifier based test-circuit to measure mismatch between transistors has been proposed in [13] but it's limited by the number of transistors that can be characterized at a time. In [3], a completely digital circuit is presented to measure local threshold voltage variations using the saturation drain current of a MOS transistor as the process-sensitive parameter. This technique suffers from an extremely low sensitivity of 0.74V/V [3]. In [14], the variation in drive-strength of NMOS/PMOS devices due to V_{th} mismatch is determined by using slew as a metric along with delay. A completely digital slew-rate monitoring circuitry in 45nm SOI is also presented. However, there is no discussion on the impact of environmental parameters on sensor-performance. A

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high sensitivity process-sensor has been proposed in [6] utilizing the extremely high process-sensitivity of MOS transistors operating in sub-threshold. However, this scheme will be extremely prone to dynamic variations (VDD and temperature) as thermal sensitivity increases by an order of magnitude when operating in sub-threshold and the sensing scheme employs no mitigation technique. Voltage and temperature independent bias generators are cumbersome and undesirable due to the area/power overhead incurred. However, a basic study of sub-threshold circuit behavior in a variable supply-temperature environment indicates that for any process-sensor utilizing sub-threshold operation, power-supply and temperature compensation is absolutely necessary to ensure reliable and reproducible measurement.

In this paper, we present a novel process sensor which utilizes the sub-threshold mode during sampling and hence, has a high resolution of 7.1V/V variation in NMOS V_{th} and a comparatively low active power consumption of 13.4µW in 45nm CMOS-SOI process. Our sensor takes advantage of the increased process sensitivity of the MOS device in the sub-threshold region of operation to allow for a higher-than-nominal sensitivity of the digitized output (325kHz/mV). The proposed process-sensor does not require any external bias or bias-generation circuitry. Instead, the process-sensitive piece responsible for threshold-voltage tracking is integrated within a VT-independent band-gap voltage-reference generator. Multiple closely-spaced devices can be characterized by using decoder-trees. We have analyzed the robustness of our design against variation in dynamic parameters – VDD and temperature, and implemented the complete sensing system in 45nm CMOS-SOI technology.

The rest of the paper is organized as follows. In section 2 we present our proposed process-sensor and discuss in detail the operation mechanism including the digitization procedure. In section 3 we perform a detailed variability analysis of our design and study the impact of variation in environmental parameters (supply and temperature) on the sensor-response. In section 4, we discuss a test-chip implementation of the proposed sensing system using a 45nm IBM-SOI toolkit provided by MOSIS. We present our conclusions in section 5.

2. Sub-Threshold Based Process Sensor

2.1 Process-Sensing in Sub-Threshold

The sub-V_{th} I_{on} has an exponential dependence on threshold-voltage as opposed to the linear dependence observed in the case of super-V_{th} I_{on}. The well-established equation used to model sub-V_{th} ON current is given as [15]:

$$I_{sub} = \mu_0 C_{ox} \frac{W}{L}(n-1)\frac{k^2T^2}{q^2} e^{\frac{(V_{GS}-V_{th})q}{n(kT)}}\left[1-e^{-V_{DS}q/kT}\right] \qquad (1)$$

where 'n' is the subthreshold slope factor ($1 + C_d/C_{ox}$) and (kT/q) is the thermal-voltage. Both current and delay variability increase dramatically in the sub-V_{th} regime due to the exponential dependence of I_{on} on V_{th}. In sub-threshold, primarily two variability sources are considered: Random Dopant Fluctuations (RDF) and Critical Dimension (CD) variations. RDF manifests itself in the form of threshold-voltage variability and hence is the dominant source of variance in sub-threshold device behavior. To illustrate the extent to which process-variability is magnified in sub-threshold we used a 15-stage ring-oscillator as a representative circuit. We modeled the threshold-voltage using an uncorrelated Gaussian distribution for the BSIM parameter – vth_0, with the standard deviation given by the following empirical model [16]:

$$\sigma_{vt} = \frac{A_{vt,RDF}}{\sqrt{WL_{eff}}} = 3.19\times10^{-8}\frac{T_{ox}N_{ch}^{0.4}}{\sqrt{WL_{eff}}} \qquad (2)$$

CD variations manifest themselves in the form of variations in effective channel-length. This we modeled using a correlated normal distribution for L_{eff} with a 3-σ of 12% on either side of the ITRS prescribed minimum value. Expectedly, the process-induced delay-spread expands drastically in sub-threshold. The 1-σ deviation increases by ~5X on moving from super-threshold to sub-threshold. Usage of long-channel, thick-oxide devices instead of nominal devices reduces the 1-σ deviation by 50% in sub-threshold. The above result motivates us to design threshold tracking circuits which utilize the sub-threshold mode of operation. The flip-side is that the sub-threshold current is extremely sensitive to temperature (exponential-dependence) and voltage variations as well. Thus, minimizing sensitivity to VT-variations is an important goal in the sub-threshold based threshold tracking circuit.

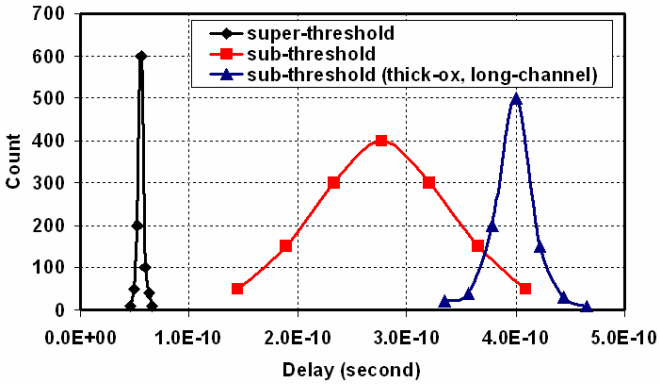

Fig 1:Delay distribution of a 15-stage ring-oscillator for different operating modes and device-types

2.2 Proposed Process Variation Sensor

The global inter-die variations present a comparatively lesser problem since from the designer's perspective, the probability of an IC to present the typical, worst or best case process-conditions is the same and the circuit is manufacturable once it meets the corner specifications. The local intra-die mismatch where the V_{th} takes on a different value on a per transistor basis requires sensing circuits for efficient tracking and to enable appropriate circuit tuning (to meet timing constraints). Our proposed process-variation sensor is designed to characterize random intra-die variations in threshold-voltage.

The basic principle of this sensor-design is based on the drain induced barrier lowering effect (DIBL). DIBL is an undesirable effect observed in short-channel devices where a high drain voltage causes the barrier height between drain and source to be lowered, resulting in a decrease in V_{th} and increase in off-state current 'I_{off}'. The reverse DIBL effect dictates that when a constant bias-current flows through a short-channel device, a low-V_{th} device develops a small drain-voltage while a high-V_{th} device develops a high drain-voltage. In our proposed design, we use short-channel transistors only for the process-sensitive piece (NMOS transistors N4 and N5). All the remaining transistors of the 1st stage are thick-oxide, long-channel and operate in the saturation region and hence, have a significantly reduced process-

sensitivity. The 2nd stage is an inverted source-follower circuit operating in sub-threshold and it provides a multiplicative factor to the process-sensitivity of the sensor.

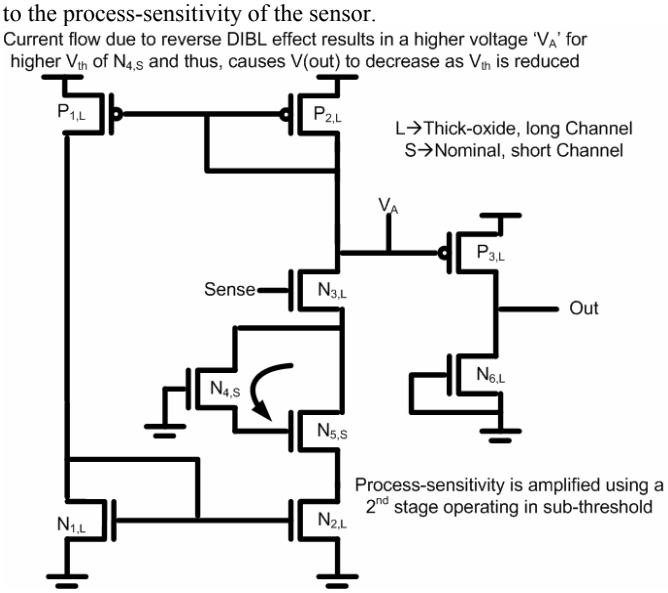

Fig 2: Process-Variation Sensor for NMOS devices

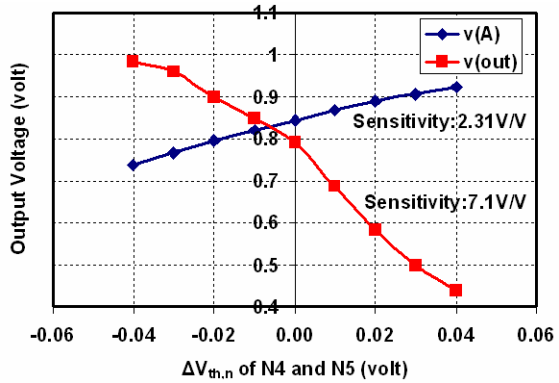

Fig 3: Sensitivity of NMOS process-variation sensor

Operation of the process-sensor is as follows: Long-channel transistors P1, P2, N1 and N2 mirror a supply and temperature independent current into the output branch of the 1st stage. The usage of thicker oxide in these transistors minimizes gate-leakage and the flow of undesirable currents in the sensing path. To activate the sensor we make the 'Sense' signal high, turning on N3 and allowing the mirrored current to flow into the process-sensitive piece. Transistors N4 and N5 are both short-channel and small in size, ensuring maximum sensitivity to V_{th} mismatch. For a high NMOS threshold voltage, due to reverse DIBL effect, drain voltage of N4 will be high and hence V_A will be high as well. When the NMOS V_{th} is low, sub-threshold leakage across N4 will cause transistor N5 to be turned ON more strongly (both due to stronger gate-bias as well as its own lesser than nominal V_{th}) which will cause the drain-voltage of N4 to reduce further and hence, reduce V_A as well. Thus, N4 and N5 form a positive feedback loop and provide magnified voltage variations to threshold variations across N4-N5. Transistor N3 operates in saturation and ensures relative temperature invariance of V_A since its own source-voltage will be lower at higher temperatures and hence compensate for any temperature-induced leakage across N4. Transistors P1 and P2 are sized in such a way that even when V_A reaches its minimum value for a very low NMOS V_{th}, transistor P3 of the 2nd stage still remains in sub-threshold. Both transistors P3 and N6 are long-channel and N6 is sized very large to maintain a large linear swing at the 'out' node. With increase in the NMOS threshold-voltage V_A increases and hence V_{out} decreases. Simulating this circuit using the 45nm Predictive Technology Model (PTM) [15] node in HSPICE, we observed a linearly increasing voltage at V_A with increase in N4-N5 threshold-voltage with a sensitivity of 2.31V/V change in V_{th}. The 2nd stage amplifies this sensitivity resulting in a much steeper slope as the sensor-output voltage decreases linearly with a high sensitivity of 7.1V for every 1V change in NMOS V_{th}. (Fig.3)

For digitization we adopted the VCO-based approach taken in the Itanium Family of processors [17] to save on area/power. Typically current starved VCOs are extremely sensitive to temperature variations and hence can potentially add noise to the process-reading during digitization. Therefore, we used the temperature-insensitive design shown in Fig.4 wherein the diode-connected transistors P_1, P_{TS} and N_1 provide temperature compensation to the remaining circuit. Transistors P_1 and N_1 were sized in such a manner that the drain current of P_{TS} remained invariant to temperature and hence, the current mirrored into the current-starved branches was also temperature insensitive. This particular VCO design offered a low temperature sensitivity of 0.0071%/ºC as opposed to a sensitivity of 0.79%/ºC observed in a regular current-starved VCO.

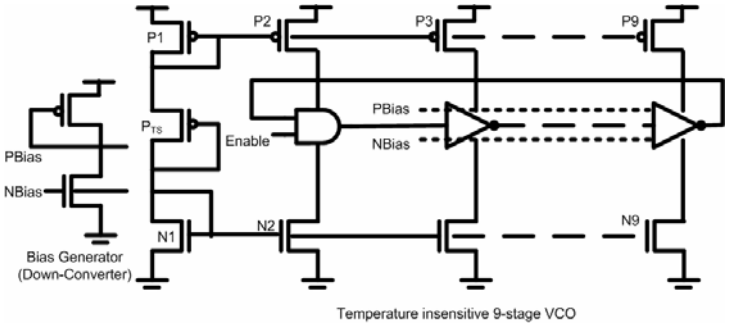

Fig 4: Digitization using temperature-insensitive current-starved 9-stage VCO (V_{OUT}=NBias)

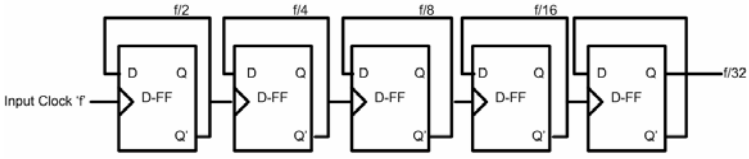

Fig 5: Divide-By-32 Ripple Divider

The sensor output served as the bias for the VCO (N-devices specifically) while bias for the P-devices was generated using a down-converter. We used a gated VCO wherein the 'sense' signal was used as the 'enable' signal and we performed digitization only when sampling the sensor to minimize power-consumption and reduce noise disturbances to other circuit blocks. The VCO frequency was converted to a digital value by using a frequency-divider (divide-by-32) (Fig.5) followed by a 10-bit counter. A simple ripple-divider comprising of five D-flip-flops was used to perform the frequency-division. Frequency-division minimizes the size of the subsequent counter needed and also minimizes chances of reflection/interference during external probing. As is evident

from Fig.3, bias for the VCO becomes weaker as the NMOS threshold-voltage of N4 and N5 increases (NBias decreases and PBias increases) and as a result, oscillation frequency of the VCO decreases linearly with V_{th} (Fig.6).We were able to achieve a relatively high post-digitization threshold-voltage sensitivity of 1.2%/mV of NMOS V_{th}. The process-sensing circuit was found to have a low active power consumption of 3.7-13.4µW while the VCO and the divide-by-32 frequency-divider have an active power consumption of 253.2µW and 318.6µW respectively in 45nm technology.

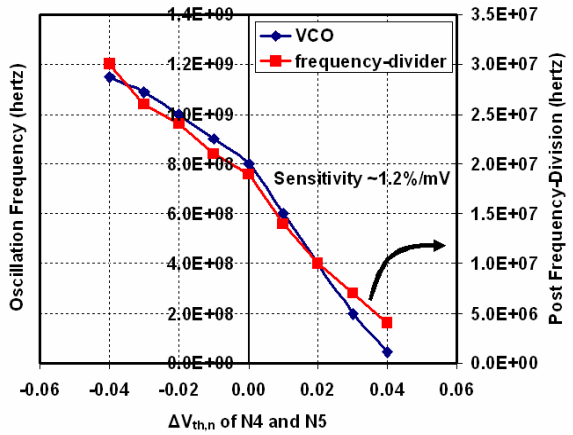

Fig 6: Digitization using VCO and frequency-divider

3. Variability Analysis of Proposed Sensor

To study the effects of intra-die threshold-voltage variations on the response of proposed sensor (both pre and post-digitization), we modeled V_{th} variations using a Gaussian distribution with a maximum variation (3-σ) of +/- 15% and performed 30 Monte-Carlo simulations. HSPICE™ (Synopsys) was the main simulation platform used in our analyses. 45nm technology files were obtained from the Predictive Technology Model website [18]. Fig.7 gives a line-histogram plot of the resultant distribution. Variability (σ/µ) of 0.014 in NMOS V_{th} was translated into a variability of 0.055, 0.071 and 0.102 at the output of the 1st stage, sensor-output and VCO output respectively (variability improvement of 4x, 6X and 8X respectively indicating progressively increasing sensitivity to V_{th} variations).

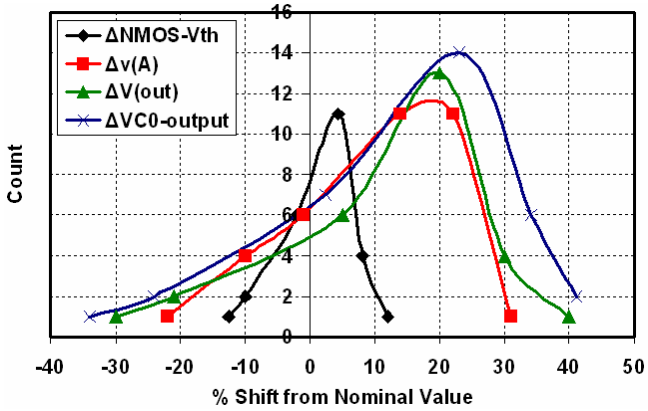

Fig 7: Histogram of % shift from nominal value of nodes at various stages of NMOS V_{th} sensing

A point of concern for process-sensors and in particular, sub-threshold-based designs is their immunity to temperature variations. It is imperative that the process-sensor has temperature sensitivity as low as possible in order to minimize the measurement error incurred due to presence of thermal gradients in the vicinity of the sensor during polling. We simulated our sensing circuit with the nominal, un-shifted threshold value and swept the temperature from 25ºC to 125 ºC. The 2nd stage increases the temperature-sensitivity of the design due to lack of any dedicated compensation circuit (0.038%/ºC from 0.015%/ºC). In spite of this increase in sensitivity, the worst-case measurement error (at 125ºC) is quite low at ~3.8%. Since the process-sensor output varies by ~0.7% per mV variation in NMOS threshold-voltage, the worst-case temperature variation will reduce the accuracy of the sensor by ~5mV of the NMOS V_{th}. This is an acceptable error since typically the sensing circuits will be used to perform process-characterization across the die in intervals of tens of milli-volts of the threshold-voltage.

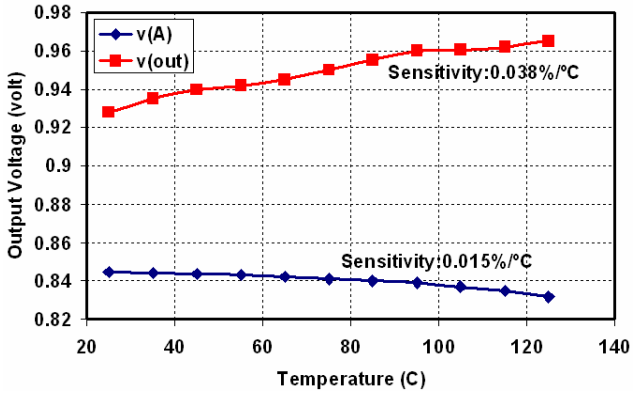

Fig 8: Process-sensor response to temperature variations

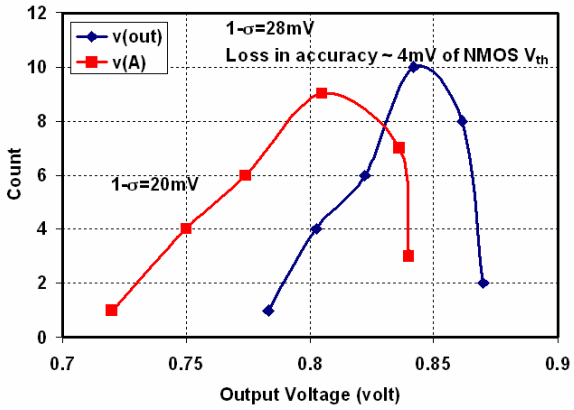

Fig 9: Histogram of sensor output in the presence of supply-noise

As CMOS feature sizes shrink and device integration density increases, on-chip power supply droop caused by large dI/dt becomes an increasing concern. To study the effect of random supply noise on sensor performance, we modeled it as a Gaussian distribution with a 3-σ variation of +/-10% (nominal supply = 1V) and ran 30 Monte-Carlo simulations. The 1-σ deviation of the sensor-output was found to be 28mV which results in a loss of accuracy of ~4mV of the NMOS V_{th} (Fig 9).

Thus, our proposed design offered a relatively high level of tolerance to dynamic variations in temperature and power-supply which is a very important design requirement for process-sensors. We varied the size of the process-sensitive transistors (N4 and N5) in our sensing circuit in order to study the impact of device-

width on deviation caused in the sensor-output voltage due to V_{th} mismatch. The deviation due to V_{th} mismatch in minimum sized devices approximates a Gaussian distribution (as seen in Fig.7). As the device-width of the process-sensitive piece is increased the standard-deviation of the spread caused by mismatch is reduced. This observation is in agreement with the proportional to $W^{-1/2}$ characteristic of threshold mismatch caused by random dopant fluctuations (RDF). The standard deviation of mismatch is further reduced when long-channel devices are used for N4 and N5 because of larger channel-area and lesser short-channel effect [13]. The standard-deviation trend with respect to device-width remains the same even with long-channel devices. Thus, short-channel, minimum sized devices for transistors – N4 and N5 provides the best sensitivity to threshold variations in our design.

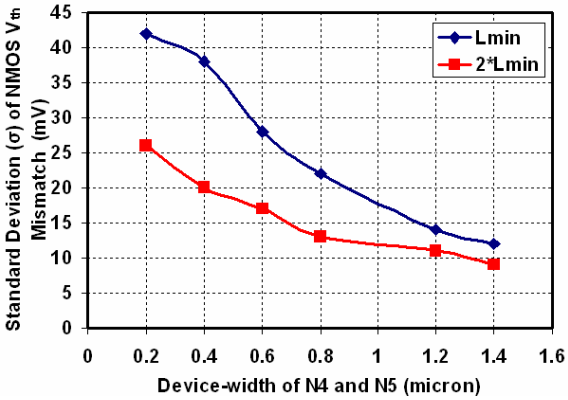

Fig 10: Impact of device-width on standard deviation of V_{th} mis-match

4. Implementation in 45nm CMOS-SOI

The proposed sensor was implemented using a 45nm CMOS-SOI design-kit provided by MOSIS. Fig.11 gives a top-level view of the complete sensing system we used in our test setup. Our test-setup comprised of 4 process-sensors which could be enabled sequentially by applying the appropriate sensor selection bits.

A 2:4 decoder and 4:1 multiplexer were used to enable and sample a particular sensor. We used separate blocks for digitization of each sensor output to minimize noise-susceptibility of the mixed-signal components. We also eliminated the counter block since off-chip measurements could easily be taken using an oscilloscope after applying appropriate buffering. A divide-by-32 frequency divider was used in order to limit the sensor-output within the MHz range. This minimizes risk of reflection observed in the GHz frequency range with meter-long probes. A cascade of buffers was used to drive the output pad. Diode-connected shunting devices were used to sink the charge accumulated during the plasma-etching process. A VDD of 1.0V was used and the sensors were sampled at 100MHz. Post-layout simulations were run to validate the design and obtain area/power results.

Our proposed design has a low area and power overhead of 45.6μ^2 and 13.4μW respectively. The entire sensing system is relatively compact at ~2400μ^2. To sample a particular sensor we apply appropriate selection bits to the decoder whose output activates the sensor as well as the corresponding VCO. The same selection bits are applied to the multiplexer as well to ensure that noise from other sensors do not corrupt the output channel and only the desired sensor-output is channeled through the I/O buffers.

Digitization using an ADC requires a large-area and also suffers from high sensitivity to different circuit parameters. In our VCO-based digitization approach, a linear mapping between sensor-output frequency and threshold-variations is maintained. Post-digitization the sensor-output has a high resolution of 325 kHz/mV variation in NMOS threshold-voltage which ensures a discernible deviation between even closely matched devices. Our VCO design is such that the shift in its gain and frequency range caused by temperature drift is nominal. Temporal averaging of the sensor-response could be used to mitigate/average-out effects of dynamic variations on sensor response. The multiple advantages of the proposed sensor include – small area, high-sensitivity, low power and high temperature/supply-noise tolerance. This is beneficial towards yield enhancement research at the circuit/architectural level since the proposed process-sensor enables fine-grain process-characterization with a low area-power overhead and the digital nature of the design eliminates the need to perform complex post-measurement data analysis thereby reducing characterization time and cost.

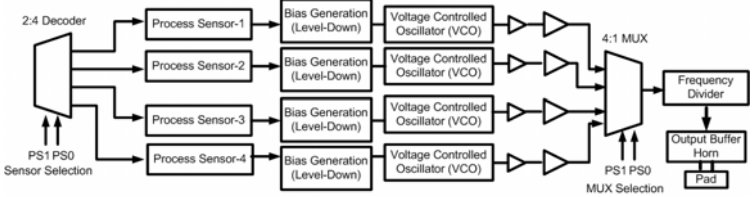

Fig 11: Test setup for proposed process-sensor using 45nm IBM-SOI toolkit provided by MOSIS

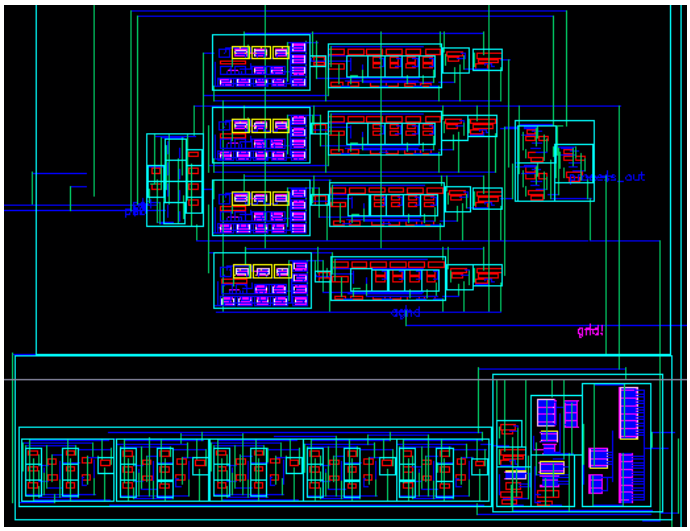

Fig 12: Layout of test-setup for process-sensors. Layers M1, M2 and M3 used for metallization. Sensors and digitization blocks are at the top while the frequency-divider and buffer-horn are at the bottom

Table 1 Area/Power overhead of sensing system at 100MhZ sampling frequency using 45nm CMOS-SOI design-kit

Component	Area (μ^2)	Power (μW)
2:4 Decoder	60.5	15.7
Process Sensor	45.6	13.4
Bias Generator	3.6	3.6
VCO	65	253.2
4:1 Multiplexer	71.2	112.5
Frequency Divider	384.3	318.6
I/O Buffers	340.5	100.4
Total	2400	897.6

Proper calibration is necessary to ensure accurate process-measurement in the presence of varying environmental parameters. Typically in analog-output process-sensors [6], the variations in sensor output-voltage are converter into ΔV_{th} using simulations. Both the measured data and simulation results are superimposed. To determine the ΔV_{th} for a measured sensor, the measured value is mapped to the closest point on the simulation curve. Effect of inter-die variations is eliminated by subtracting $\sigma(\Delta V_{th})$ from each data-point and hence normalizing the data for the particular die.

For digital designs [3] the VCO frequency is calibrated against threshold variations by using a device to drive the VCO whose gate is externally controllable. The VCO frequency is measured for a series of gate-voltages and a one-time calibration-table is prepared based on the premise that each small change in the device gate-voltage corresponds to a certain amount of V_{th} shift. The IV-characteristics of the controlling gate might vary from one sensor to another and hence, the same calibration table cannot be used for all the process-sensors distributed across the die.

Thus, for usage in actual microprocessors, a more prudent approach will be to follow the calibration procedure used in the Itanium family of processors for thermal-sensing [17]. The method can be applied to process-sensors as well by using a temperature-compensated, precision band-gap voltage reference to cycle the VCO through a fixed set of voltages and create a frequency/output-count to voltage mapping table. Henceforth, any frequency/output-count reading will lie between two particular points in the calibration-table constructed previously and the corresponding ΔV_{th} can be obtained by interpolation (enabling higher resolution).

Table 2 Comparison with state-of-the-art designs

Sensor	Power	Area	Sensitivity/ Resolution	Process
[6]	-	-	7.05V/V	65nm Bulk
[13]	-	-	10mV	130nm Bulk
[3]	-	$150\mu^2$	0.74V/V	45nm SOI
[14]	-	$1575\mu^2$	0.95MHz/mV	45nm SOI
This Work	13.4μW	$45.6\mu^2$	7.1V/V 325kHz/mV	45nm SOI

5. Conclusions

A digital CMOS process sensor targeted for on-die process-characterization with high tolerance to temperature variations and supply noise was implemented in 45nm CMOS-SOI technology. Due to utilization of sub-threshold mode of operation, the design offers a high NMOS threshold-sensitivity of 7.1V/V at the output and a post-digitization sensitivity of 325 kHZ/mV. The design has a low active power consumption of 13.4 μW and an area overhead of $45.6\mu^2$. The use of predominantly digital and mixed-signal components ensures a compact layout measuring $2400\mu^2$ for the entire prototype sensing system. The design exhibits good tolerance towards temperature variations and supply induced noise, incurring an accuracy loss of 5mV (worst-case) and 4mV (1-σ) respectively for a sampling frequency of 100MHz.

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