Impact of Clock-Gating on Power Distribution Network using Wavelet Analysis

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***Abstract*—With the extensive use of clock-gating in modern microprocessors to reduce the power consumption of the chip, it is imperative to analyze the effect of clock-gating on the Power Distribution Network (PDN) and how it affects the voltage drop across the grid. This paper presents a methodology to generate a set of synthetic gating patterns given a power grid, information about how the grid is loaded and regions that belong to different clock-gated domains. Wavelets are used to generate the initial voltage responses as they envelope both the frequency and time domain enabling us to capture frequency information of the PDN to analyze and generate a time-domain signal (voltage drop). The responses generated are then input to a Linear Program (LP) that outputs the worst-case clock-gating patterns and maximum voltage drop at the point of interest. The results show the worst-case gating patterns and the associated voltage drop at a particular point of interest for a set of clock-gated domains. This methodology finds applications in verification of the integrity of the PDN and individual blocks and also, is useful for test pattern generation.**

***Index Terms*—Power Distribution Networks, Clock-Gating, Voltage drop, Wavelet Analysis, Linear Programming**

I. Introduction

The robustness of Power Distribution Networks (PDN) is vital for the correct operation of all the chip modules in a modern microprocessor. The continuous scaling of transistors and the rapid increase in their operating frequencies contribute to the major sources of noise for the PDN [1]. This precipitates the need for analyzing PDNs in an efficient and accurate manner, as the PDNs themselves also become more complex which leads to computational issues.

Much work has been done in analyzing the two forms of noise on the power lines, namely, IR drop from the RC elements of the power grid and the simultaneous switching noise (L*di/dt* drop) due to the parasitic inductances of the chip and packaging. The voltage drop across the grid may worsen if the noise input excites the grid's natural resonance frequency. Hence, it is imperative for any analysis to consider the resonance aspect as well.

Clock-gating has become a major feature in the modern VLSI design as the increase in the size of the Clock Distribution Network (CDN) needed to provide proper clocking to all the clock dependent modules in the chip also led to the CDN consuming a larger portion of the total chip power ($\sim 30 - 50\%$) [2]. Various methods of introducing clock-gating into a given design have been explore. In [3] the authors describe a method to introduce both clock and power-gating and tabulate significant reduction in power consumption in presence of clock-gating for various ISCAS '89 circuits.

While clock-gating provides significant reduction in the power consumption of the CDN, certain gating patterns may excite the resonance impedance of the power grid which will lead to a large voltage drop. This is due to the large transient currents that occur when the region of interest switches in and out of gating and the PDN experiences the sudden change in the current loads.

In this work, wavelet-based technique is used to generate a worst-case clock gating pattern to maximize the voltage drop at a point of interest at a given time. Wavelets are used as the main components of the analysis as they envelope both the time and frequency domain simultaneously [4] and provide an efficient tool to analyze the voltage drop on a PDN. This can be used as a form of feedback for designing of the modules that are present at any particular point of interest as the analysis can use the global information about other modules present on the die to find the local effects due to clock-gating. Wavelets are created by extracting the relevant information from the PDN impedance profile. Then, the wavelets obtained can be used to generate a set of voltage responses at a point of interest. These responses are then fed into a Linear Programming (LP) formulation to maximize the voltage drop at the particular point.

The remainder of this paper is organized as follows: Section II describes some of the related work in this area. Section III explains the mathematical framework of the wavelets and the preliminaries for the LP formulation. Section IV describes proposed design flow. Section V describes the experimental setup and lists the results obtained. Section VI describes possible scenarios for application. Finally, Section VII concludes this paper.

II. Prior Work

Wavelet based analysis of a power grid has been extensively carried out in [4]. The authors use a wavelet transform to generate current stimuli which represent active loads to the grid, and use them to determine the worst-case voltage drop

at a particular point on the grid using a LP formulation. In this work, we extend the authors' analysis to include the effect of clock gating and use the LP to extract the worst-case gating patterns for each unique clock-gated domain.

The effect of clock gating on the PDN and extraction of worst-case clock-gating patterns has been studied in [5]. The authors convert the current waveform into the frequency-domain and then, use a vector fitting method to obtain the voltage response in the time domain. Next, an algorithm is used to extract the worst voltage variation and the corresponding gating patterns. The use of wavelets in our work results in the generation of voltage response from a set of basic current loads composed of wavelets. These loads are synthetic and can be modeled to optimize the simulation time in a circuit simulator, like HSPICE. The LP is then used to generate the worst-case gating patterns. Real-time knowledge of the circuit operation needs to be encoded only in the LP stage.

The work in [5] focuses on using LP for predicting a voltage violation and is built on the work in [6] and extended to a 3D domain. The main focus is finding the time and amount of violation and gating patterns that resulted in the violation. The LP in this work differs from [5] in the formulation of the constraints. In [5] the constraints for the LP are based on the voltage responses with the gating variable and the objective function maximizes the violation time and amount of violation in voltage. In our work, the constraints only deal with the current waveforms which include the gating variables and the objective function maximizes the voltage drop at a particular node and time [4].

III. Mathematical Framework

In this section, we cover the key mathematical constructs and their use in this work. Wavelet analysis is useful for capturing the temporal variation of voltage drop by utilizing the frequency-domain information of the current loads and the power grid itself (impedance). Next, the preliminaries for the LP formulation is explained where the process of including the gating information is shown.

A. Wavelet Analysis

Wavelet transform allows any function, either periodic or non-periodic, to be represented in terms of a set of basis functions (Wavelets). Conversely, a set of wavelets can be used to construct synthetic waveforms with desired shape. The impedance response of the power grid can be used to construct the wavelets so that they capture the relevant frequency information.

The simplest form of a wavelet is a Haar wavelet [7] and is shown in Fig. 1. The discrete time equation for the Haar wavelet is given in (1). A wavelet can be manipulated in two ways: it can be moved along the time-axis denoted by time shift parameter and it can be stretched or squeezed based on the wavelet scale.

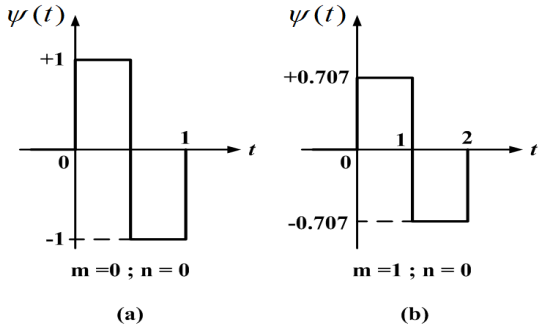

Figure. 1: **Discrete Haar Wavelet Examples**

$$\Psi_{m,n}(t) = \frac{1}{\sqrt{2^m}}\Psi\left(\frac{t-2^m n}{2^m}\right) = A_m\Psi(2^{-m}t-n) \quad (1)$$

where $A_m = 2^{\frac{-m}{2}}$ is called the amplitude of a wavelet at scale m and n represents the number of shifts from time t by unit time, 2^m.

Each wavelet is centered around a center frequency, f_c = 2.33/($\pi 2^m$) [7]. The number of such wavelets to use can be found from the impedance profile of the power grid where we find the frequency region of interest and using the lower and upper frequencies (f_{min} and f_{max}, respectively) the value of m_0 (the largest scale which also is the total number of scales) is given by (2). The value of m_0 is floored and the wavelets are constructed using $m = 1, 2, ..., m_0$. m = 1 is used to represent the shortest (or fastest) wavelet while $m = m_0$ represents the longest wavelet (or slowest).

$$m_0 = \left\lfloor log_2\left[\frac{2f_{max}}{f_{min}}\right]\right\rfloor \quad (2)$$

Let *u* represent a unit time constant for the wavelet analysis (equal to half the period of the fastest wavelet) and is given by (3).

$$u = \frac{2.33}{2\pi f_{max}} \quad (3)$$

The set of Haar wavelets obtained can considered as band-pass filters [7] and provide a finer resolution for analysis of the power grid whose impedance response is used to set the frequency region of interest. This form of Multi-Resolution Analysis (MRA) can be used to construct loads that excite the power grid impedance within the frequency bounds. An example of MRA using Haar wavelets is shown in Fig. 2 where we have $m_0 = 3$ and normalized frequency region of interest is between 0.1 and 1. Here, the Scaling Function (m=3) provides an approximation for the impedance response of the power grid below f_{min}.

The Haar wavelet is used in this work because the current loads are constructed as Piecewise Linear Waveforms (PWLs). The set of basis wavelets that are constructed from the impedance profile of a power grid can be used to create a current load which is represented by (4) [4].

$$i(t) = i_{dc} + \sum_{m=1}^{m_0}\sum_{n=1}^{n_m} T_{m,n}\Psi_{m,n}(t) \quad (4)$$

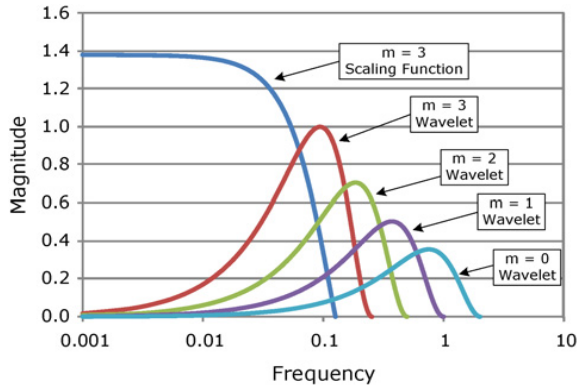

Figure. 2: **MRA using Haar Wavelets [4]**

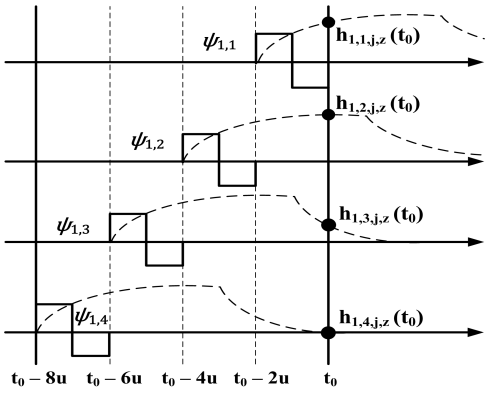

Figure. 3: **Shifted wavelets and their response**

where i_{dc} is used as an approximation that accounts for the current stimuli from all the frequencies below f_{min} and $T_{m,n}$ represents the weights or detail coefficients [4] that are used to construct the required waveform *i(t)* around an offset of i_{dc}.

B. Linear Programming Preliminaries

Since the effect of clock-gating on the PDN needs to be analyzed, we need to include a gating variable when constructing the synthetic current source. The LP is then formulated so that we find the gating pattern while maximizing the voltage drop at a particular point. Equation (4) can be modified to include the gating term and the result is given by (5).

$$i_j(t) = i_{min,j} + \sum_{p=1}^{t_0/u}(1-\alpha_p)\sum_{m=1}^{m_0}\sum_{n=1}^{n_m} T_{m,n}\Psi_{m,n}(t) \qquad (5)$$

where $i_j(t)$ represents the j^{th} current source, t_0 is the time at which the voltage drop needs to be maximized, p is an index used to represent the time windows which are of unit size *u* and the number of such windows in which the current source can either be gated or non-gated is given by t_0/u (t_0 is assumed to be a multiple of *u* for simplicity), α_p represents a binary variable and is explained in (6).

$$\alpha_p = \begin{cases} 1 & \text{unit is gated} \\ 0 & \text{unit is not gated} \end{cases} \qquad (6)$$

Lastly, $i_{min,j}$ represents the leakage current when the j^{th} module that is assigned the current load $i_j(t)$ is clock-gated. This is because we know that a clock-gated block will only consume leakage power.

A point to note is the term $\alpha_p T_{m,n,j}$ in (5) represents a non-linear term for the LP as both variables need to be optimized to obtain the final results. But, knowing α_p is a binary variable we can work around it by describing separate sets of constraints for each value of α_p. There are various methods to do this and in Section IV we explain the method used in this work. Thus, since α_p is essentially an integer the entire formulation now constitutes a Mixed Integer Programming (MIP) model. This subsection of the LP model is what we solve to obtain the final results.

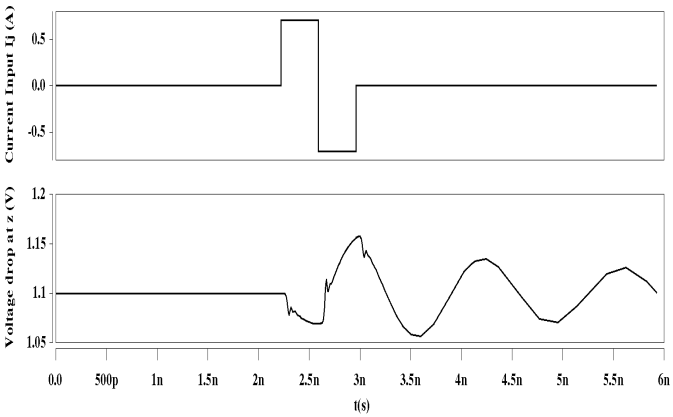

Figure. 4: **Voltage response at *z* from current load at *j***

IV. Design Flow

The general steps in the design flow are explained as follows:

Obtain Impedance Response: A power grid is generated and the impedance profile of the grid is found. This profile is needed to construct the set of basis wavelets that are to be used to create the synthetic current sources.

Calculate the wavelet parameters: Once we specify the frequency region of interest, f_{min} and f_{max}, in the impedance profile of the grid we can calculate m_0 and *u* from (2) and (3) in Section III-A. Also, t_0 can be specified (should be equal to the slowest wavelet time-span or greater).

Generate the voltage response at point of interest: The power grid is loaded with current loads, the number of which can be specified by the designer. For generating the voltage drop response at the point of interest from each current load ($i_j(t)$), the current waveforms are assumed to be a set of pulse inputs with pulse-widths dependent on *m* and *u*; and shifted backwards in time from t_0 [4] and the response, denoted by $h_{m,n,j,z}(t0)$, is found each time. Fig. 3 illustrates the shifted wavelets and their corresponding responses. Fig. 4 shows an example of a response at some point of interest, *z*, from a single current load (j = 1,m = 1) at node *j*, considering an actual PDN.

Solving the LP: The set of responses from the previous step for each of the current sources can be optimized as some of the time shifted wavelets produce a zero voltage drop at the point of interest (eg. response from input $\Psi_{1,4}$ at node z, $h_{1,4,j,z}(t0)$, in Fig. 3 is zero) and these inputs can be discarded to speed up the LP solving. Also, at this stage, we input the relevant data like the leakage current values for each of the loads, the power constraints which decide the maximum current that is drawn by a load and the clock-gated regions information. Further information can be provided by a designer for generating more detailed constraints to make the analysis relevant to design under consideration. The LP formulation is explained in detail in Section IV-A.

A. LP Formulation

In this section, the Objective Function and the constraints for the LP formulation are described. Given this formulation, we can maximize the voltage drop at a particular point, z.

1) Objective Function: Given the voltage drop responses, the objective function calculates the maximum voltage drop at the target location at a specific time, t_0. Let $v_{z,j}(t_0)$ be the voltage drop at point z due to the current load at *j*. The drop is given by (7) [4].

$$v_{z,j}(t_0) = d_j imin, j + \sum_{m=1}^{m_0} \sum_{n=0}^{n_{m,j}} h_{m,n,j,z}(t_0) T_{m,n,j} \quad (7)$$

where, d_j is the voltage drop at z when a current load of 1A is present at node *j* and $h_{m,n,j,z}(t_0)$ is the voltage response from a current load with stimulus $\Psi_{m,n}(t)$.

The objective function is given by the summation of all the voltage drop responses from all current stimuli, considering there are *q* stimuli in total. This is represented in (8).

$$v_z(t_0) = \sum_{j=1}^{q} v_{j,z}(t_0) \quad (8)$$

2) Constraint Generation: The effect of clock-gating can be mathematically encoded in the form of constraints. Given (5) and knowing that $\alpha_p T_{m,n,j}$ is non-linear and cannot be solved directly by the LP, we come up with a set of constraints to simulate the product $\alpha_p T_{m,n,j}$. For each of the current loads we can separate the waveform into time-slots of width *u* and write the constraints for each slot, *p*. This is given by (9).

$$0 \leq \sum_{m=1}^{m_0} T_{m,n,j} \Psi_{m,n,j}(t) \leq (1 - \alpha_p)(i_{max,j} - i_{min,j}) \quad (9)$$

where, $\Psi_{m,n,j}(t)$ can be either A_m or $-A_m$ or 0 (in case the wavelet is not present in the time slot), $i_{max,j}$ is the maximum current that the particular load consumes. Equation (9) provides the bounds for the wavelets that are part of the current load and specifies whether the current load is gated in a particular time slot, *p*.

The above constraints consider all the current loads to be under different clock-gated regions. But, we can group the constraints for current loads in the same clock-gating domains and assign the same α_p to them.

Other constraints can be generated depending on more detailed designs which can further increase the accuracy of the results. Some examples are defining the bounds for $T_{m,n,j}$ using power traces [4] and also, we can specify constraints for the gating patterns themselves. In this work, the LP allows a module to shift between clock-gated and non-gated phase in every unit time window.

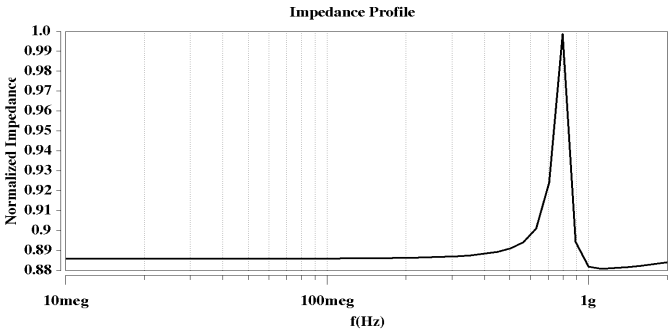

Figure. 5: **Impedance Profile of the Power Grid**

TABLE I: POWER GRID SPECIFICATIONS

Technology Node	45nm
Metal Layers Used	M2, M3
Physical Die Dimensions	1mm x 1mm
Grid Size (Nodes)	40 x 40

V. Experimental Setup and Results

A simple two metal layer power grid was considered to analyze and verify the methodology. The specifications of the power grid that was used for this work are listed in Table I. Using these specifications, the impedance profile is found and is shown in Fig. 5.

Given the impedance profile, the frequency range of interest is taken as f_{min} = 200 MHz and f_{max} = 1 GHz. This gives m_0 = 3 and u = 0.37ns. We take the time at which to maximize the voltage drop as t_0 = 5.92ns. This gives us a total of 16 timeslots.

To obtain the current load values we considered a unit load block to consist of an AES circuit taken from [8] which was synthesized using Synopsys Design Compiler and Nangate Open Cell Library. Power analysis was done using VCS and Primetime-PX. The effective size of the AES block covers 5X5 nodes and consuming a peak power of 80mW and a leakage power of 0.3mW. Considering a voltage supply of 1.1V this gives us the current bounds as i_{max} = 72.727mA and i_{min} = 0.27mA for the one unit block. For analysis, we assume that the center of the block has the current load. To create the unique clock-gated regions, the unit block is instantiated multiple times and spread arbitrarily into 10 unique clock-gated regions. Each region is assigned an α and all the current loads within that region are controlled by this α. A total

TABLE II: WORST-CASE GATING PATTERNS

Region	Pattern
1	0011001101100110
2	0011001100110110
3	0000000100010000
4	0011001101100110
5	0000000100010000
6	0011001101100110
7	0000000101000000
8	0011001101100110
9	0000000101000000
10	0011001100110110

TABLE III: VOLTAGE DROP AT POINT OF INTEREST Z

	Voltage Drop (mV)
From LP	176
From SPICE	164

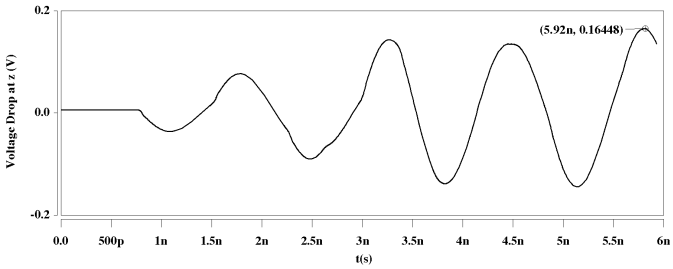

Figure. 6: **Voltage Drop waveform at point of interest, z**

of 39 such blocks are spread between the 10 gated regions considered which gives a total power budget of 3.2W for the grid (this is below the 4-8W/mm2 power budget generally considered to be the maximum [9]). One of the grid corners which is farthest from all the loads is taken as the point of interest.

Considering the above specifications, the LP formulation is solved using a solver like GLPK which yields the gating pattern for the 10 uniquely clock-gated domains shown in Table II. Table III lists the voltage drop obtained at the point of interest at time t_0 using the LP. Using the values of currents in each time-slot obtained from the LP we run SPICE simulations and find the maximum voltage drop. This is also listed in Table III.

Fig. 6 shows the voltage drop waveform at the point of interest, z, from all the current sources at time t_0=5.92ns as obtained from SPICE.

To verify that the obtained gating patterns are the worst we consider 10,000 sets of random patterns. Each set consists of 10 16-bit random patterns which are assigned to the current sources in the uniquely gated domains and this used as the basis to run SPICE simulations to obtain the maximum voltage drop at z during the time period 0 to t_0. Fig. 7 shows the plot of the voltage drops along with the drop obtained from our

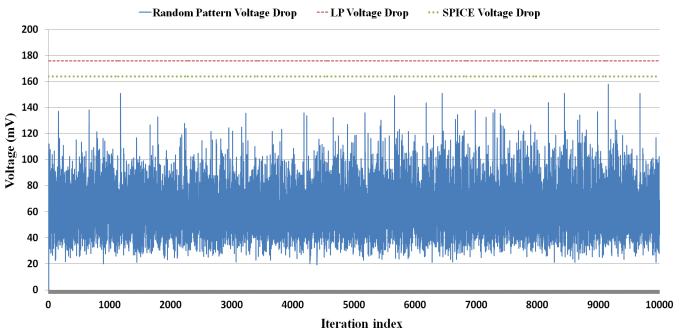

Figure. 7: **Voltage Drop Comparison**

methodology for comparison. We see that the LP formulation produced voltage drop is much larger than the ones obtained from the random sets and produces this drop at the specified time t_0.

The above results show that the methodology developed can be used to obtain the maximum voltage drop at any point on a power grid at any time of our choosing. Extension to real power grids will involve more data points and a greater set of constraints can be included to model the behavior of the current loads to match real-world settings.

VI. Applications

There are many possible scenarios where this work would be relevant and the methodology can be applied. Two such applications are listed below.

During the early design phase of a processor a Power Grid Designer can use this formulation to quickly verify/redesign a grid given general power budget for various blocks and provide feedback to the groups working on the blocks about the gating patterns that would affect their respective blocks and also, about the noise levels observed at various locations of interest.

In the final stages of processor design, Test Engineers can use the formulation to generate test vectors and also to test critical paths in the design. Multiple points of interest can be defined along the path and weighted according to relevant constraints like delay sensitivity to noise and the analysis can be run considering all the points to generate one set of gating patterns that will affect the critical path delay the most.

VII. Conclusion

We present a methodology to extract the worst-case clock-gating patterns and the associated voltage drop that is introduces due to clock-gating at a point of interest in the power grid. Wavelets are used for analysis and an LP is formulated to generate the worst gating patterns and the worst voltage drop. This information is essential for creating robust designs which operate in a clock-gated regime. The results show the clock-gating patterns and the worst-case voltage drop waveform for a particular point on the grid and verify the worst-case voltage drop using random enumeration of gating patterns.

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